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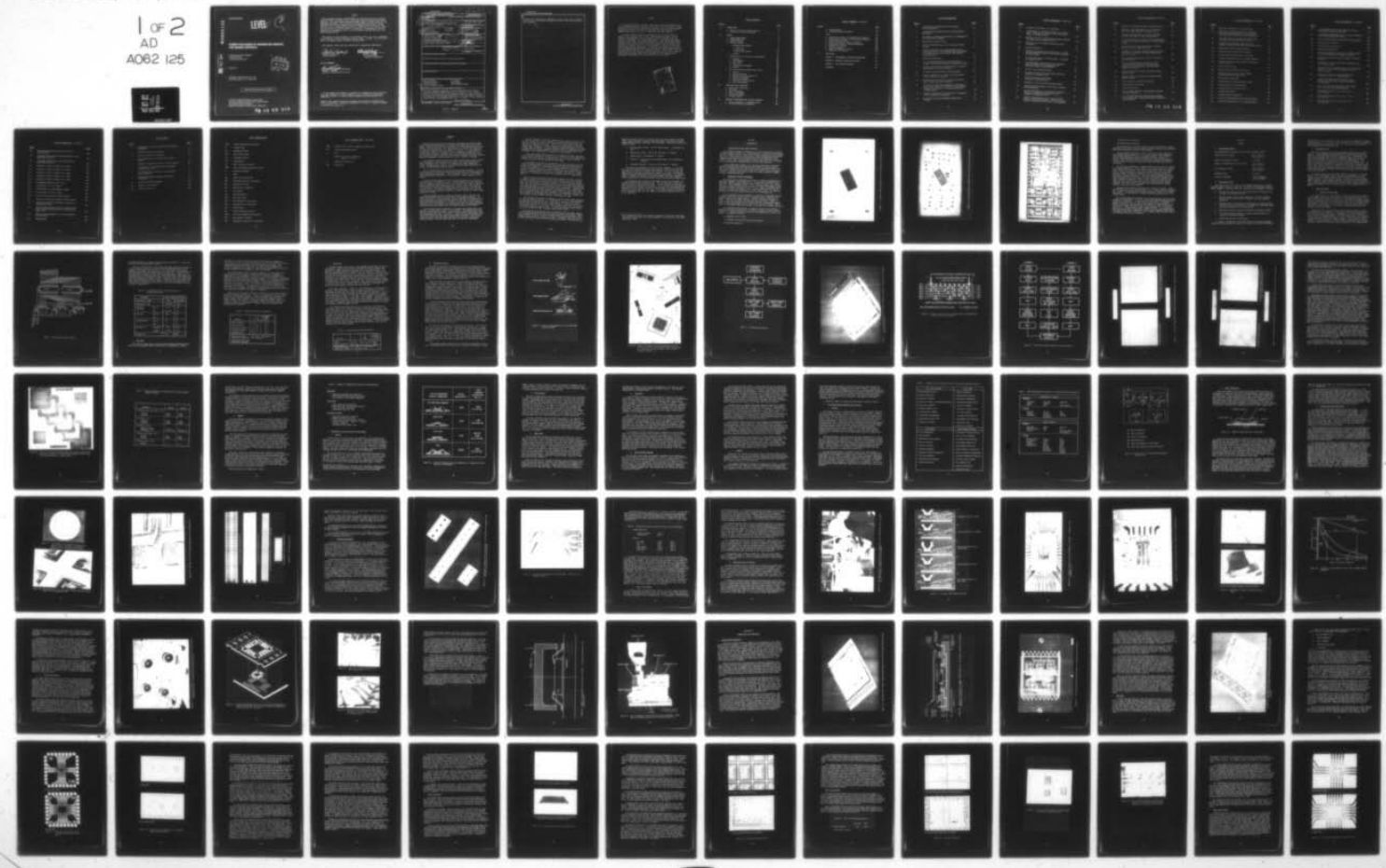

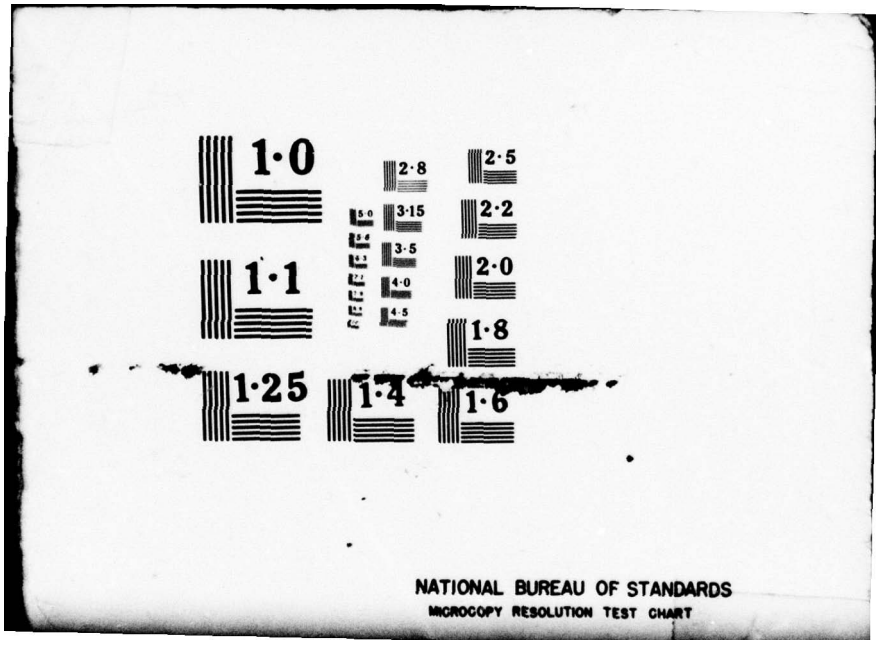
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LEVEL II

HYBRID PACKAGING OF INTEGRATED CIRCUITS FOR ENGINE CONTROLS

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This technical report has been reviewed and is approved for publication.

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This report documents the design, test, and development of an advanced electronic packaging candidate for future, on-engine electronic controls. Materials with low and well-matched expansion properties, special processes, and special joining alloys were used because of the large number of thermal cycles expected. Tape-automated bonding was used because it offers improved reliability and lower production cost.

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Included in the program were temperature cycling, thermal shock, vibration bench testing, and on-engine environmental testing. The results obtained were favorable.

PREFACE

This report describes a design, fabrication, and testing program on hybrid assembly technology conducted by the General Electric Company and sponsored by the Air Force Aero Propulsion Laboratory, Air Force Systems Command, Wright-Patterson AFB, Ohio under Project 3066 Task 306603 and Work Unit 30660369 with Charles E. Ryan, Jr., AFAPL/TBC as Project Engineer.

The work reported herein was performed during the report period of August, 1974 to January, 1978. Ray E. Anderson was the General Electric Company Program Manager, and the technical work was performed under the direction of Howard B. Kast, Engineering Manager. The Engineering Manager wishes to thank James A. Loughran and Dominic A. Cusano of the Power Module and Hybrid Unit, General Electric Corporate Research and Development Center and Robert P. Wanger, Daniel J. Frey, and Edward L. Gollar of the Aircraft Engine Group for their assistance. In addition, the authors wish to gratefully acknowledge the benefits derived from helpful informal discussions with key engineering personnel of CII Honeywell Bull, St. Ouen, France. They are grateful also for the innovative contributions made in the use of Kovar for tape-automated bonding (TAB) tapes by personnel of AMP Incorporated at Harrisburg, Pennsylvania and at Winston-Salem, North Carolina.

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LIST OF ABBREVIATIONS

CITS	Central Integrated Test System
CP	Ceramic Plane
DF	Dissipation Factor
DIP	Dual Inline Package
IC	Integrated Circuit
I/O	Input/Output
Hz	Hertz (cycles per second)
JTDE	Joint Technology Demonstrator Engine
K	Dielectric Constant
k	1000
LSI	Large Scale Integration
MMI	Monolithic Memories Incorporated
MP	Metallization Plane
MSI	Medium Scale Integration
pF	Pico Farads
ppm	Parts Per Million
ROM	Read Only Memory
RTV	Room Temperature Vulcanizing
SEM	Scanning Electron Microscope
S/N	Serial Number
SIC	Silicon Integrated Circuit
SSAO	Solid State Applications Operation
TAB	Tape Automatic Bonding
TCR	Temperature Coefficient of Resistance

LIST OF ABBREVIATIONS (Concluded)

THTD	Transient Heat Transfer Temperature Distribution
TTL	Transistor-Transistor-Logic
W	Watts
α	Thermal Coefficient of Expansion ($cm/cm/°C \times 10^{-6}$)
ΔT	Temperature Difference
$\Omega/\square$	Ohms/Square

SUMMARY

Modern aircraft gas turbine technology advancements may require engine control functions which alter or reconfigure the engine operating cycle in flight. These new functions imply the presence of additional actuators which increase control complexity. As a consequence, the circuitry and complexity of electronic engine controls are likely to increase. It is most important to maintain or improve on the high levels of reliability characteristic of current control systems. Although solid state electronic techniques offer the potential for good reliability, the increased complexity of future controls makes the achievement of high reliability levels a distinct challenge.

The electronic control on an aircraft gas turbine faces a severe temperature environment. This environment can produce life-limiting electronic package degradation due in part to the numerous wide range temperature cycles. Package failure, fatigue, and metallurgical/chemical/corrosion are a few of the difficulties that can result.

Here a new microelectronic hybrid package has been evaluated. It introduces design features which provide special capabilities for withstanding the engine temperature environment. This development is based on the concept of utilizing materials selected for a close match of thermal expansion coefficients.

The major design objective for the selected approach was to develop an inherent ability to withstand as many as 36,000 temperature cycles successfully (although no attempt was made to log this many test cycles). Materials, bonding procedures, and joining alloys were chosen to meet this objective. The substrate is alumina with tungsten runs and Kovar pins. The leads and cover are Kovar. The technical approach was to use materials with low and well-matched thermal expansion properties, thereby reducing the stress during temperature cycling.

Hybrid packaging entails a higher heat density than is found in the widely used printed circuit board and dual-in-line-package approach. Advances were made in the hybrid module design to minimize the temperature difference produced by transferring this heat from the chip to the heat sink. This required the development of a thermally efficient heat path through the thickness of the chip bonding alloy and substrate into an aluminum mounting bracket and down the bracket to the fuel-cooled chassis on the bottom.

Test prototype hybrid assemblies, using memory and counter chips, were designed and fabricated to serve as test vehicles. Developmental-type problems were encountered with some of the new fabrication and processing steps, and advancements were made, This hybrid package utilizes large square interfacing pins rather than the smaller conventional round pins. The selected vendor developed special brazing techniques which provided strong pin-to-substrate joints. Pin bend tests were used to verify this achievement.

Thermal expansion coefficient objectives led to the use of Kovar leads. In order to use Kovar, it was necessary to develop bonding, etching, and plating techniques to replace the conventional processes which have been historically employed with copper. Much of this development was done experimentally, leading to a Kovar-to-polyimide bonding technique, an etching process, and tin plating. A special adhesive system was developed for Kovar accommodating the thermal expansion coefficient which is much lower than polyimide - 5.0×10^{-6} cm/cm/° C versus 20.0×10^{-6} cm/cm/° C.

Unique tape designs were developed to accommodate the wider edge bevel that is produced during the etching of Kovar. This need arises because, when etching Kovar, more material is removed laterally for a given thickness (lower etch factor) than is experienced with copper.

Electroless tin plating of lead materials is most critical to the subsequent joining processes. New fabrication steps have been introduced to provide this capability. Experimental evidence shows that Kovar will not accept electroless tin plate. A new development by AMP Incorporated, a supplier to this Program, resulted in a new catalytic plating bath having a specific formulation which may be used to deposit a thick layer of copper onto Kovar. Electroless tin plate then was applied over the copper-plated Kovar.

Most of the conventional microelectronic hybrid, those which are made by companies without an in-house silicon chip capability, utilize "flying leads" in connecting the semiconductor chips to the substrate metallization. When used, such leads are a major consideration in the reliability apportioning. With the objective of building more circuitry into each hybrid package, it becomes necessary to pretest the chips prior to attachment. Otherwise the hybrid assembly manufacturing yield will be unacceptably low. These needs led to the selection of tape-automated bonding (TAB) or cinema film carrier as the method for making lead and chip bonds. The advantages of TAB include chip availability by accommodating existing devices, good heat transfer, low cost assembly, and performance testing of chips while on tape.

Gold plating the chip pads or bumping is the first step toward preparing the chips for lead attachment. This consisted of a series of sputtering and plating steps using several metals. Gold plating the memory chip pads in this program, the General Electric Company modified an existing process for putting this metal on the chip pads. The resulting process was successful as is verified by the zero loss of chips. The process requires a mask, which, in case of the memory chips, was made from the wafer itself.

These various processes were used in building a total of eight complete hybrid assemblies having materials with matched thermal coefficients. These test specimens served as a basis for demonstrating the microelectronic hybrid package through a series of functional tests. Functional large scale integration (LSI) memory devices were metallurgically bonded to the substrate and

served as the test vehicle* for evaluating the package integrity including bonds, interconnections, conductor runs, and leads. These hybrid packages demonstrated successful performance and environmental capacities through this series of tests:

- Pin attachment flexure - two 90° reverse bends - 2 substrates (76 pins)
- Temperature cycling - 300 cycles, 600 hours - 4 hybrids
- Thermal shock - 50 exposures - 4 hybrids
- Vibration - 20 g's, 0.04 inches peak-to-peak, 50 to 2000 Hertz - 4 hybrids
- On-engine endurance - 30 hours and 23 minutes - 4 hybrids

The tests were performed in the above listed sequences. It is recognized that microelectronic hybrids have relatively high resonant-response frequencies by virtue of the small sized elements. In fact, the most damaging engine vibrational frequencies are known to fall above the frequency range of currently applicable military engine specifications. Consequently, special attention was applied to accurately measure the actual vibration levels encountered at the chassis/engine interface during the on-engine runs.

Accelerometers were mounted to the chassis during this on-engine test. Triaxial vibration was recorded on tape. Data were obtained at four fan speeds from 40% to 100% rated (7570 rpm). It was found that predominant fan duct vibratory excitations corresponded to the first-stage fan blade passing frequency of 50 per revolution and to a second-stage fan blade passing frequency of 88 per revolution. The range of excitating frequency recorded was 10 to 10,000 Hertz and, over this range, the maximum recorded value was 10 g's at 4400 Hertz.

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*After assembly and prior to the hybrid evaluation, the devices - MMI 5086 - were found to have come from a wafer incapable of operating over the engine temperature range.

SECTION I

INTRODUCTION

1. Need for Electronic Engine Controls

The probable increase in complexity of the next generation of military aircraft engines is expected to lead necessarily to the use of full-authority electronic engine controls. This level of engine complexity and the expanding need for more complete aircraft/engine control integration forces a commensurate increase in the complexity and required capability of the control system. This increased control system capability must be obtained with requisite safety, responsiveness, precision and stability.

Digital electronics appears to be the most viable means of meeting these significantly more sophisticated requirements of future engines. With its inherent ability to "time share" in the computational section of the control, increasing requirement complexity yields a very much smaller increase in hardware (and, hence, failure rate) when compared to present control system mechanizations.

2. Advantages of Hybrid Packaging

Reliability can be improved by reducing the number of components in an electronic assembly. More extensive use of large scale integrated (LSI) and medium scale integrated (MSI) silicon integrated circuit (IC) devices does this. Fewer components require fewer connections among them, thereby contributing further toward better reliability. Fewer IC components do not necessarily require less space, though, because conventional LSI and MSI packages are larger and inefficiently consume mounting area. In some, the active silicon IC chip occupies less than 2% of the package area.

Hybrid integrated circuit assemblies, consisting of unpackaged silicon IC chips mounted and interconnected on a passive ceramic substrate, are deemed attractive for engine controls. Hybrids have many advantages to offer. First is their small size and good space efficiency. Figure 1 shows the 30:1 size reduction obtained by replacing a conventional printed circuit board logic assembly with a functionally identical hybrid. The 1-inch x 2-inch ceramic substrate contains 31 IC chips and 6 ceramic capacitors.

A conventional analog assembly is compared in size with its hybrid functional equivalent in Figure 2. The hydrid assembly is shown in detail in Figure 3. The two-conductor-layer-thick film substrate is 1 inch x 2.15 inches. The assembly contains:

21 Integrated circuit chips

7 Precision thin-film-on-silicon-chip resistors

25 Thick film resistors

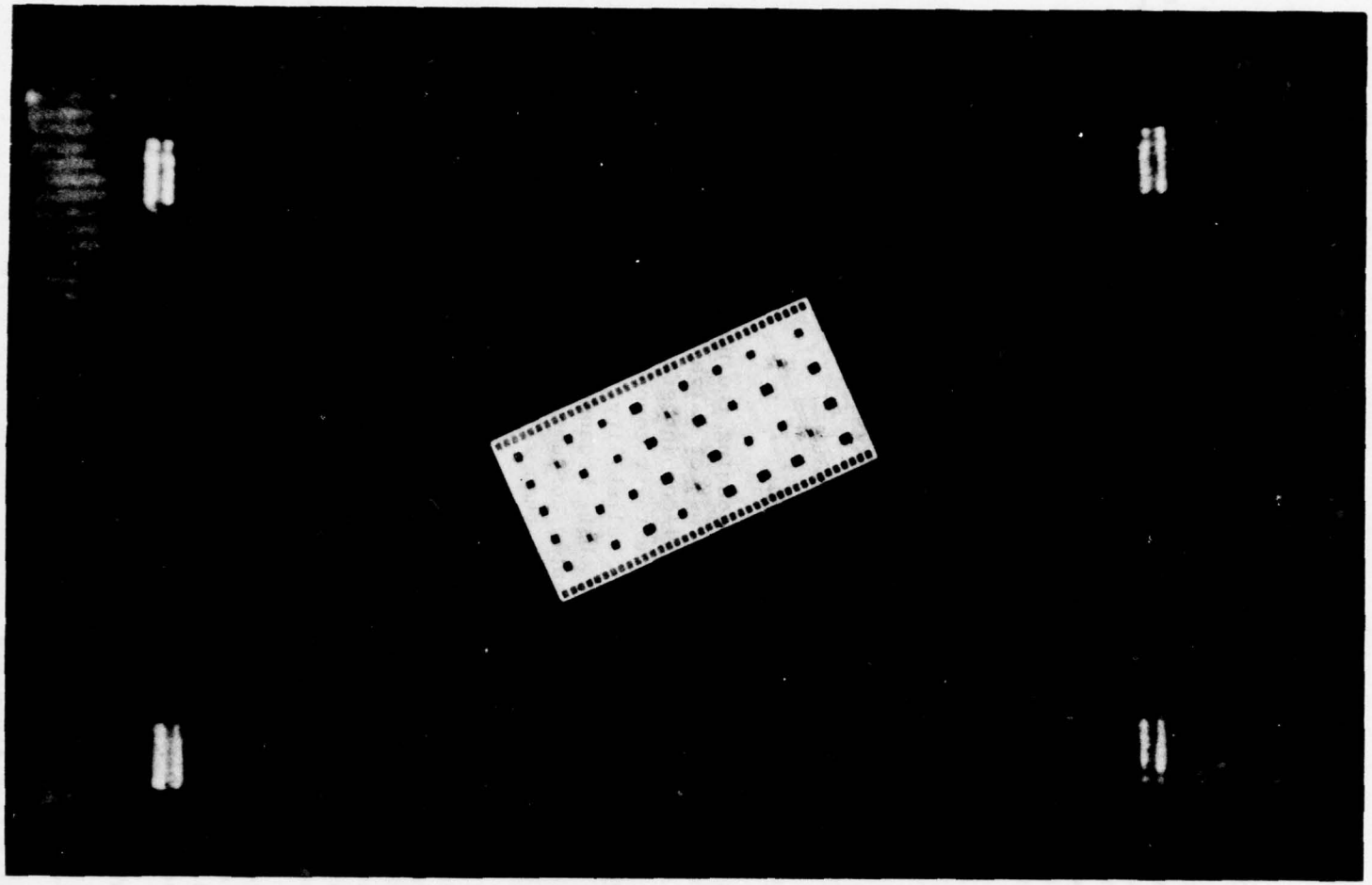


Figure 1. A Digital Hybrid Substrate with its Printed-Circuit Equivalent.

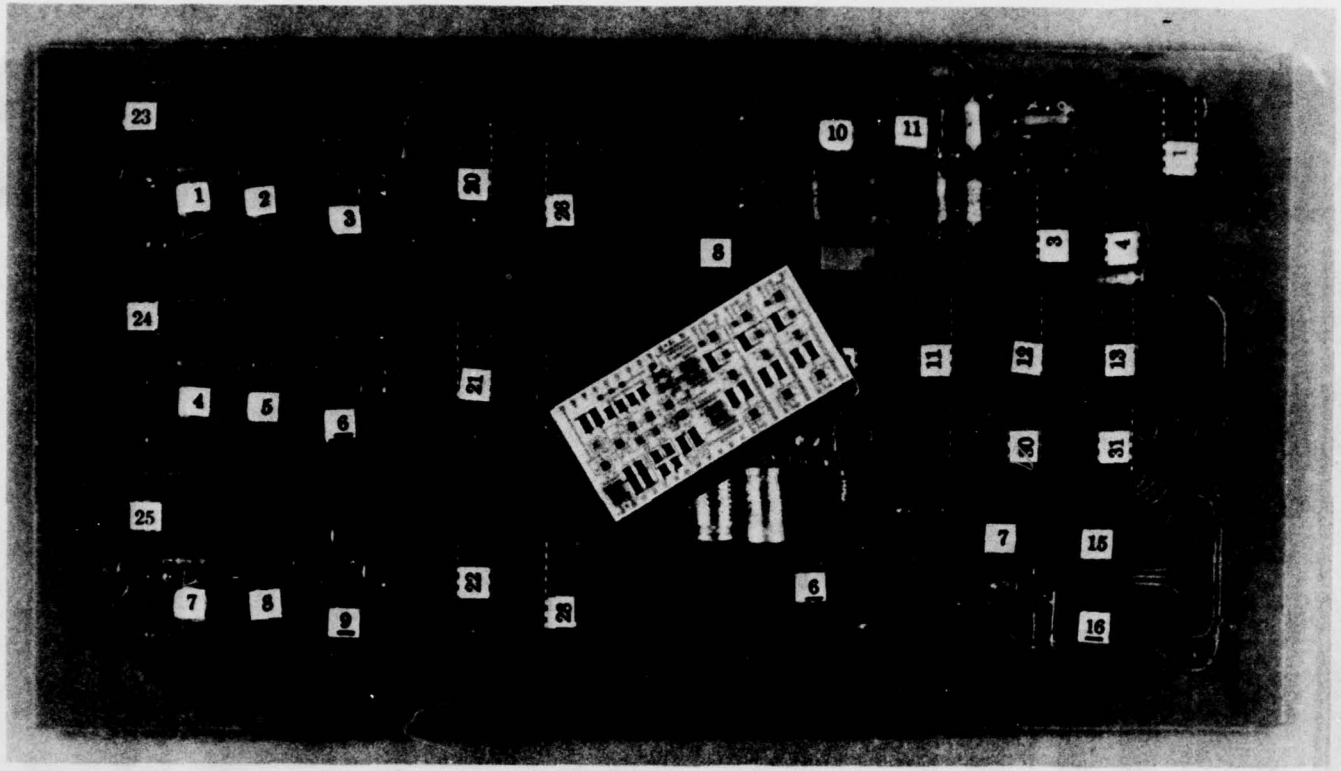


Figure 2. An Analog Hybrid Assembly with its Printed-Circuit Equivalent.

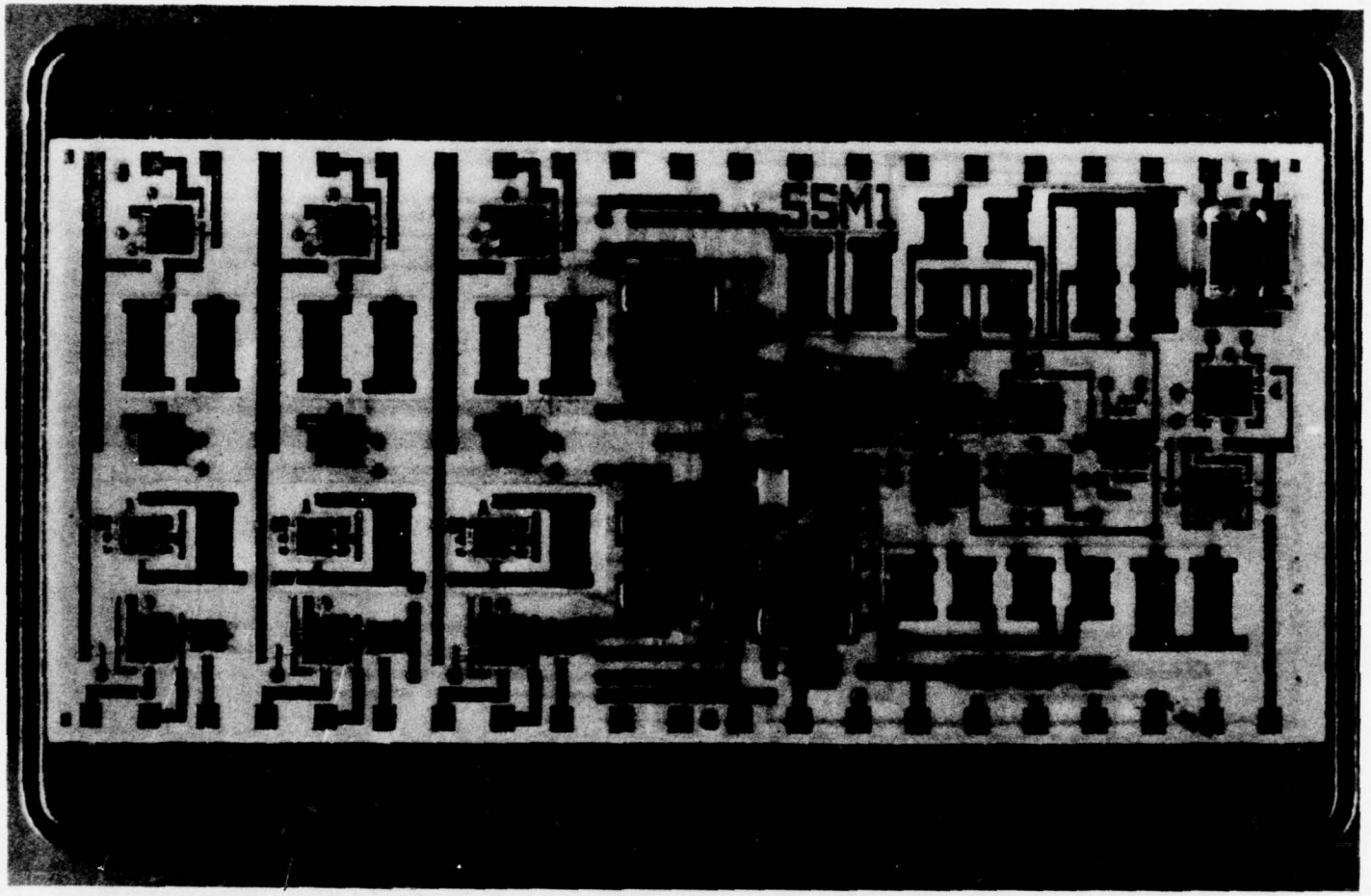


Figure 3. Two Layers of Conductors Interconnect 63 Components in the Analog Hybrid Assembly.

10 Ceramic chip capacitors

256 Wire-bonded connections

The printed-circuit and hybrid assemblies shown in Figures 1, 2 and 3 were made at the General Electric Company Corporate Research and Development Center for projects not related to this program.

Interconnection substrates are batch fabricated at high temperature using stable inorganic materials. As a result, hybrids offer tolerance to the elevated temperatures used for assembly processes. The use of a ceramic substrate provides good heat transfer from the attached silicon devices. Fewer soldered connections usually are required with hybrid substrates because the internal connections already have been made by batch processing.

The electrical performance of digital hybrid circuits often is superior to classical equivalents. Fast IC chips can be closely spaced in a manner which reduces the inductance and parasitic capacitance of the interconnections. This provides better logic pulse fidelity and faster rise times. The short signal transmission distance within the hybrid decreases the propagation time and eliminates the need for matched impedance connections with their resistive terminations. The functionally dense hybrids, with their concomitant small size, greatly reduce the number of printed circuit boards required in equipment. This, in turn, improves reliability with fewer connectors and the associated logic pulse reflection and ringing problems. The overall result is higher logic operating speed, reduced crosstalk, and better noise immunity.

Hybrids provide flexible packaging with a variety of options. Almost any substrate size can be selected; sizes to 5 x 7 inches have been demonstrated. A variety of package sizes, shapes, and types is available to enclose the assembly. In some designs, the hybrid substrate becomes a part of the package itself.

For a hybrid fabrication process to be a practical one, it must fulfill a number of requirements. It must be operable in a manufacturing environment rather than a laboratory. It must have the flexibility to accommodate a variety of circuits, large or small, and in small to large quantities. It should be producible and reproducible and should offer ease of fabrication. It must have a high yield and it must be cost effective for its intended application. It should employ simple assembly methods. Of paramount importance for complex hybrid assemblies, it must offer in-process repairability of assemblies and should provide for fully automated 100% electrical test of all component parts prior to assembly.

SECTION II

DESIGN

1. Design Requirements

The environmental requirements for the hybrid assembly include:

Temperature Cycle Range	−67° to 257° F (−55° to 125° C)
Number of Temperature Cycles	to 36,000
Ambient Air Temperature at Control Unit	−54° to 470° F (48° to 244° C)
Fuel Temperature Range	−65° to 210° F (−54° to 99° C)
Vibration Level	to 20 g's
Acoustic Environment	150 dB maximum at 100 to 10,000 Hz

2. Design Objectives

The primary objective of this hybrid packaging program was to improve on-engine digital control reliability. To achieve this reliability improvement, a number of technical steps were identified for development, including:

- Reducing the number of parts and interconnections through the use of Large Scale Integration (LSI).
- Reducing thermal stress during temperature cycling by using materials with low coefficients of expansion and less expansion difference.
- Reducing junction temperatures by decreasing the temperature drop incurred from chip to substrate, from substrate to mounting bracket, and from the bracket to the cooling fluid.
- Improving vibration resistance through better mechanical design.
- Increasing inherent hardness by avoiding tin-lead solder and plastics in the hybrid package.
- Eliminating the use of flying leads.

In regards to reliability, the failure rate goal for hybrid packaged digital control assemblies for engines as complex as the JTDE is 20 failures

per 10^6 hours. It is necessary to keep the chip ambient temperature substantially less than 257° F for satisfactory reliability. As a goal, a temperature drop from chip to cooling fluid of 10° F was selected for heat loads of 1 watt per square inch of substrate area.

3. Selected Circuit

The circuit selected for the hybrid assembly demonstration is shown by Figure 4. The two memory chips (MMI 5086) were obtained from Monolithic Memories, Incorporated and contain the sine function. These memory chips were selected because they are LSI in complexity level; similar chips, in dual-in-line-packages (DIP's), were successfully temperature cycled in excess of 3000 cycles at General Electric in an earlier program. The memory chip size is 0.150 inch by 0.171 inch, and it has 24 lead pads. The three counter chips (93S16) were obtained from Fairchild Camera and Instruments. The counter chip size is 0.080 inch by 0.108 inch. Both the memory and counter chips have aluminum metallization, while the Fairchild counter chips were delivered by the vendor with gold-plated bumps over the aluminum interconnection pads.

The circuit shown includes the major devices (or chips) of a program memory. The program memory provides the data and commands for a digital engine control. The memory chips are Read Only Memories (ROM's) which average 500 gates. The mechanical design is identical to customer program ROM's required by digital engine controls. The three counters are Medium Scale Integration (MSI) devices which average 50 gates. These binary counters provide the program counter (P-counter) function which addresses the LSI ROM's.

4. Substrate Design

a. Substrate Technologies

The hybrid assembly of this program consists of a number of unpackaged silicon integrated circuit chips mounted on a supporting structure. The same structure also contains the electrical interconnections among the chips as well as those going to the outside world. Also the structure may contain other features which allow it to become an integral part of a sealed protective package. Alternatively, the structure can be enclosed within an independent separate package. The structure is commonly known as the substrate of the hybrid assembly.

The goals of the hybrid packaging program imposed a number of unique requirements upon the substrate. Ultimately, the technology selected must have the longer range capability of accommodating 50 to 100 integrated circuit chips in a single assembly. This will require from 3 to 6 conductor layers over areas approaching 20 square inches. Moderately high conductor resolution will be required to achieve adequate circuit density. The materials of construction must be closely matched in expansion coefficients to minimize thermally induced stress within the assembly. The substrate must

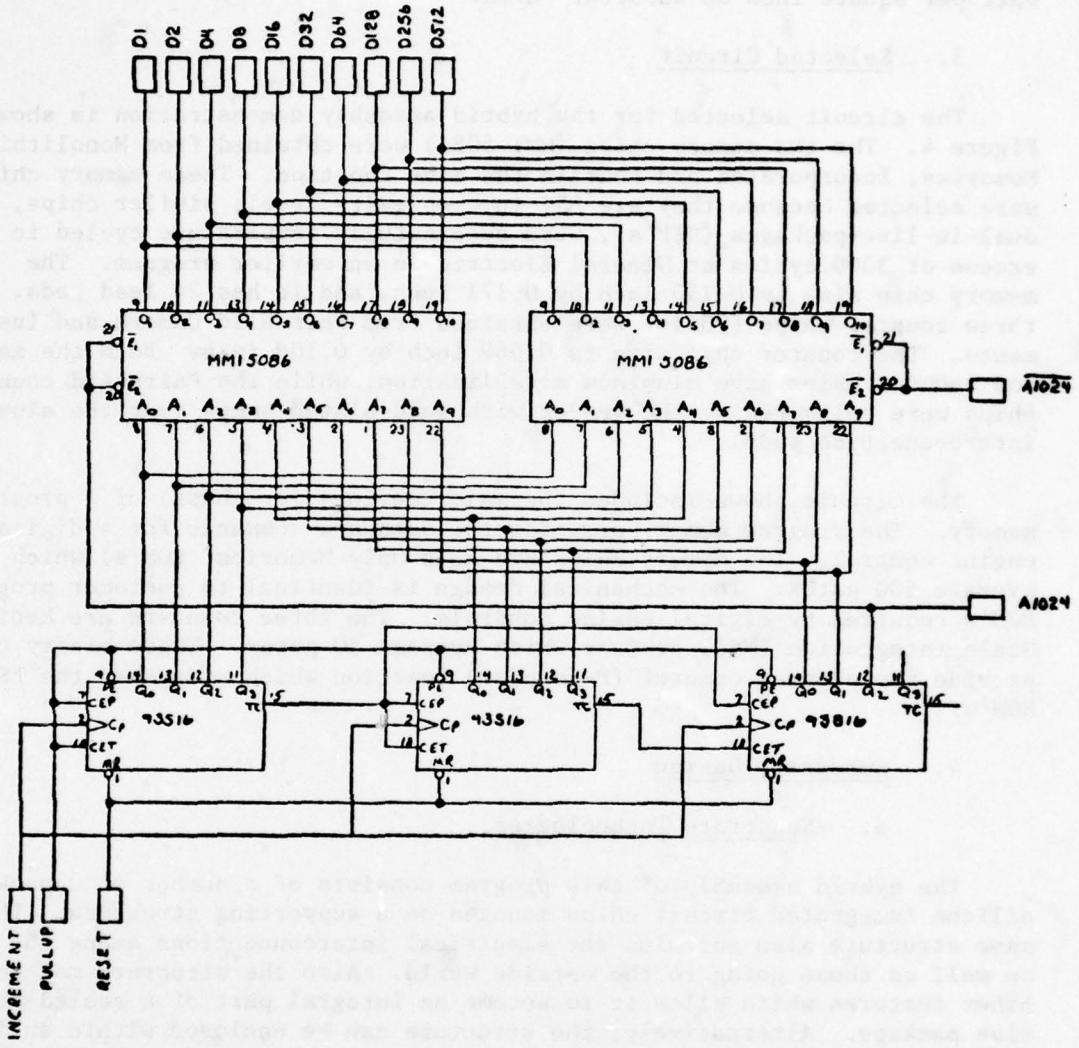


Figure 4. Hybrid Module Memory Circuit.

be rugged and immune to damage caused by assembly operations. It must also survive the many temperature excursions.

Crucial to the success of this hybrid packaging program was the need to select a substrate which would satisfy both the interconnection and the packaging requirements and constraints. Many approaches to fabricating hybrid substrates have been demonstrated in recent years. Some have been of fleeting interest because of cost, processing complexity, yields, lack of repairability, or similar deficiencies. Only three hybrid technologies have attained wide-spread acceptance as viable, practical ones: thin film, thick film, and multilayer monolithic ceramic. These three substrate technologies were reviewed carefully for their ability to satisfy the program needs. A comparison of the capabilities of thin and thick film technologies is shown in Table 1 (Reference 1).

Table 1. A Comparison of Thin Film and Thick Film Process Capabilities.

Parameter		Thin Film	Thick Film
Resolution, inches		<0.001	0.003-0.005
Resistivity, Ω/□		100-2000	1-100M
Stability (per Year)	typical	<0.1%	<0.5%
	best	few ppm	0.1%
TCR, ppm	typical	<100	<200
	best	<5	<50
Tracking, ppm	typical	<10	<50
	best	1	10
Tolerance, %	processed	±5-10	±10-30
	trimmed	to 0.01	to 0.1
Dielectrics		few	many

1. Thin Film

Thin film is a high vacuum technology that transports materials from a bulk source and deposits them as a thin film on the substrate. Typical

depositions are less than 50 microinches thick, hence, the designation "thin" film. Usually the deposited layers cover the entire substrate surface and subsequently are patterned by photolithographic processing. Some materials, dielectrics in particular, also can be pattern-deposited by placing a patterned stencil mask near the substrate and allowing the material to pass through only the openings to reach the substrate.

Thin film networks exhibit excellent capability for high resolution - narrow lines and close spaces - because photolithography is employed. Dimensions of a few thousandths of an inch, or less, are attainable with good yield and close tolerance. Resistors made in thin film can be exceedingly stable but are limited to a narrow range of values. The available dielectric materials are very limited, and even simple crossovers are difficult to process with acceptable yields. Thin metallic layers make assembly difficult, especially with solders. Often the metallic layers must be thickened by subsequent electroplating. Although starting with low cost bulk materials, thin film requires complex and expensive vacuum equipment which has relatively low productivity, making it an expensive technology.

There are very few useful dielectrics available in thin film technology, as shown in Table 2 (Reference 1). Their use is limited to very thin layers which have low breakdown voltages. Dielectric deposits have numerous pinholes in them, causing frequent short circuits between conductor layers. Simple crossovers are difficult, requiring complex processing. There is no process in thin film capable of providing the multilayer interconnection substrates needed for the program. Therefore, the use of the thin film technology was eliminated.

Table 2. Thin-Film Dielectric Properties.

Material	K	% DF 1 kHz	Voltage** Strength (2000 Å)
Silicon Monoxide	~6	0.1	35 V
Silicon Dioxide	4	0.04	35 V
Tantalum Pentoxide*	~25	1.0	40 V
Titanium Dioxide*	~50	0.5	25 V
Aluminum Oxide*	~9	1.5	25 V
Capacitance Range: 3×10^4 to 6.5×10^6 pF/in.^{2} Temperature Stability: 35 to 800 ppm/° C *Anodized metal films **Void-free specimen			

2. Thick Film

The more popular thick film is a less demanding technology for fabricating hybrids. Passive interconnection networks are made on ceramic substrates by a simple sequence of printing and air-firing operations. Commerically available pastes are deposited on the substrate in patterns by printing them through stencil screens. When heat treated at elevated temperature, the pastes are converted into high quality conductors, resistors, and dielectrics. The finished prints vary from 0.0005 inch to 0.002 inch in thickness - much thicker than those of the thin film technology and, hence, the designation "thick" film. A wide variety of pastes is readily available to satisfy nearly all hybrid requirements. Many pastes employ noble metals to allow the air firing. Although initially expensive to purchase, the pastes are used efficiently and circuit costs are low.

Thick film technology is ideal for volume production of interconnection networks. This technology is based on screen printing which is a room environment process that uses simple, highly productive equipment. It is a very versatile and flexible process providing dense networks with conductor widths and spaces as small as 0.005 inch. Stable resistors are available over a wide range of values - a few ohms to many megaohms. Tolerances to 1% are easily and economically attained with laser trimming. Dielectric layers easily accommodate electrical crossovers, and multilayer conductor structures are common. A judicious choice of conductor materials optimizes the network for a solder-oriented assembly process.

The preferred thick film dielectrics for multilayer interconnection substrates, Table 3, are derived from glass technology (Reference 1). Because these dielectrics are glassy in nature, a low tensile strength results, and the dielectric must be compressively loaded in practice to prevent cracking. The thermal expansion of these materials is designed deliberately to cause the substrate, upon cooling down from processing temperature, to generate a compressive force within the dielectric layers. Until the very recent introduction of new, better matched dielectrics, significant substrate warpage could be created by thick film dielectric layers. It was the thermal expansion mismatch that prevented using the then-available thick film dielectrics for this hybrid program.

Table 3. Thick Film Dielectric Properties.

Material	K	% DF 1 kHz	Voltage Strength (2 mils)
Glass	4 to 10	0.1 to 1.0	~600 V
Devitrified Glass	8 to 20	0.1 to 2.5	~600 V
Ferroelectric	50 to 2000	0.5 to 5.0	~300 V
Capacitance Range: 1.5×10^3 to 3×10^5 pF/in.^{2}			
Temperature Stability: ±25 ppm to ±30%			

3. Multilayer Ceramic

The need for improved environmental protection of packaged discrete semiconductor devices led to the development of ceramic-based device enclosures. As the semiconductor devices became more complex, so did the ceramic packages. The so-called "green tape" process, sketched pictorially in Figure 5, was developed to facilitate the economical fabrication of complex ceramic packages like those of Figure 6. The green tape technology is now a mature one, capable of both protecting and interconnecting a multiplicity of semiconductor devices with a single monolithic ceramic structure.

These structures are fabricated by first preparing individual sheets of thin, flexible, unfired ceramic tape. Figure 7 outlines the process. Ceramic powders, typically alumina, are mixed with solvents and a fugitive thermoplastic binder to form a slip or slurry. The mixture then is cast or extruded to a desired thickness. When dried, the resulting sheet is tough and flexible, superficially resembling a sheet of plastic film. Since all ceramics exhibit a significant shrinkage as they densify during their high temperature firing, it is important to predict and control this shrinkage in the tape process. This is done by test firing a sample of each lot of tape produced to ensure the correct shrinkage. A qualified lot of tape then is cut into convenient size pieces for subsequent processing.

A completed assembly employing a multilayer monolithic interconnection structure is shown in Figure 8. One hundred flip-chip integrated circuits are assembled on a 1.4-inch-square ceramic substrate which contains five internal and two surface layers of metallization. The cross section is shown schematically in Figure 9. A series of six individual green tape layers was prepared for laminating. Each layer was provided with a group of holes, or vias, which, when filled with a tungsten metallization, served to provide electrical continuity through the layer. The same tungsten metallization also was printed on the surface of each tape layer in an appropriate pattern. The conductor pattern was printed over the via, already filled with metallization, to continue it through the tape to the next layer. The above assembly was designed and fabricated for a General Electric Company project not related to this program.

The process flow sequence is illustrated in Figure 10. Tape for each layer is cut into two-inch-square starting blanks, Figure 11(a). A gang tool simultaneously punches into a tape blank all the 0.008-inch-diameter via holes required for that layer, along with alignment holes in the four corners. Figure 11(b) shows the punched tape for layer CP1 of the illustrative assembly. A total of 1381 via holes were punched simultaneously with the alignment holes. Next, the via holes are filled by printing the tungsten metallization ink over the vias. A mild vacuum exerted through the vias during printing pulls in the ink to completely fill the vias, as shown in Figure 12.

The required conductor pattern then is printed on the surface of the tape. Where printed over the filled vias, electrical continuity is carried

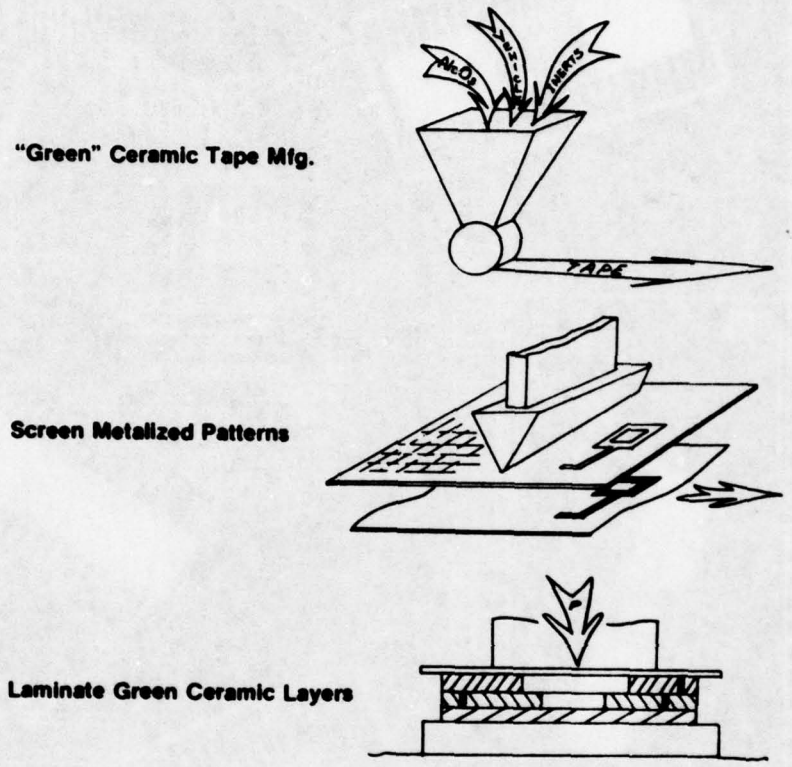


Figure 5. Pictorial Representation of the Green-Tape Ceramic Process.

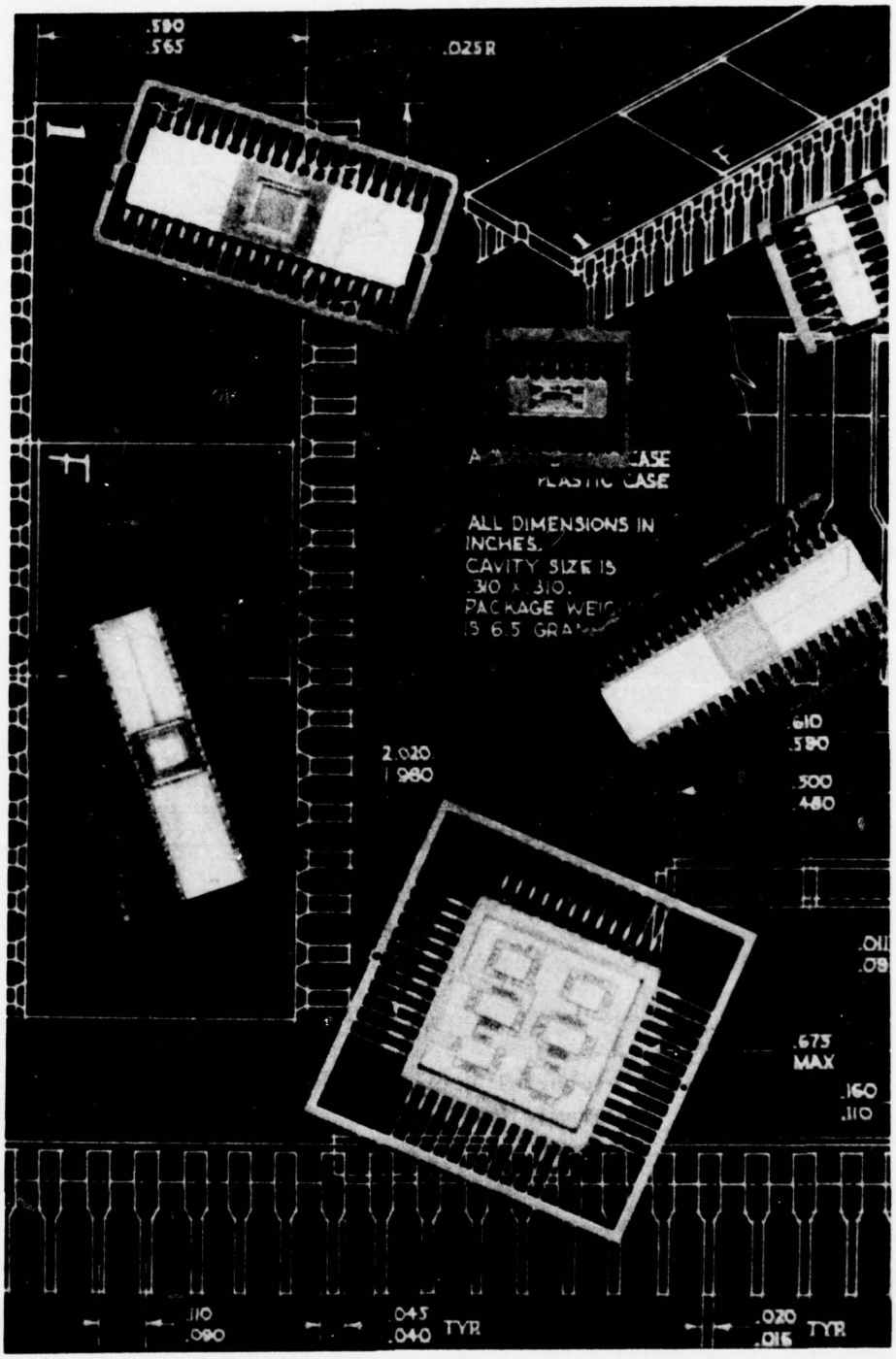


Figure 6. Ceramic Integrated Circuit Packages Made with the Green-Tape Process. The Bottom Package Interconnects Six Integrated Circuits by Means of Two Internal Conductor Layers.

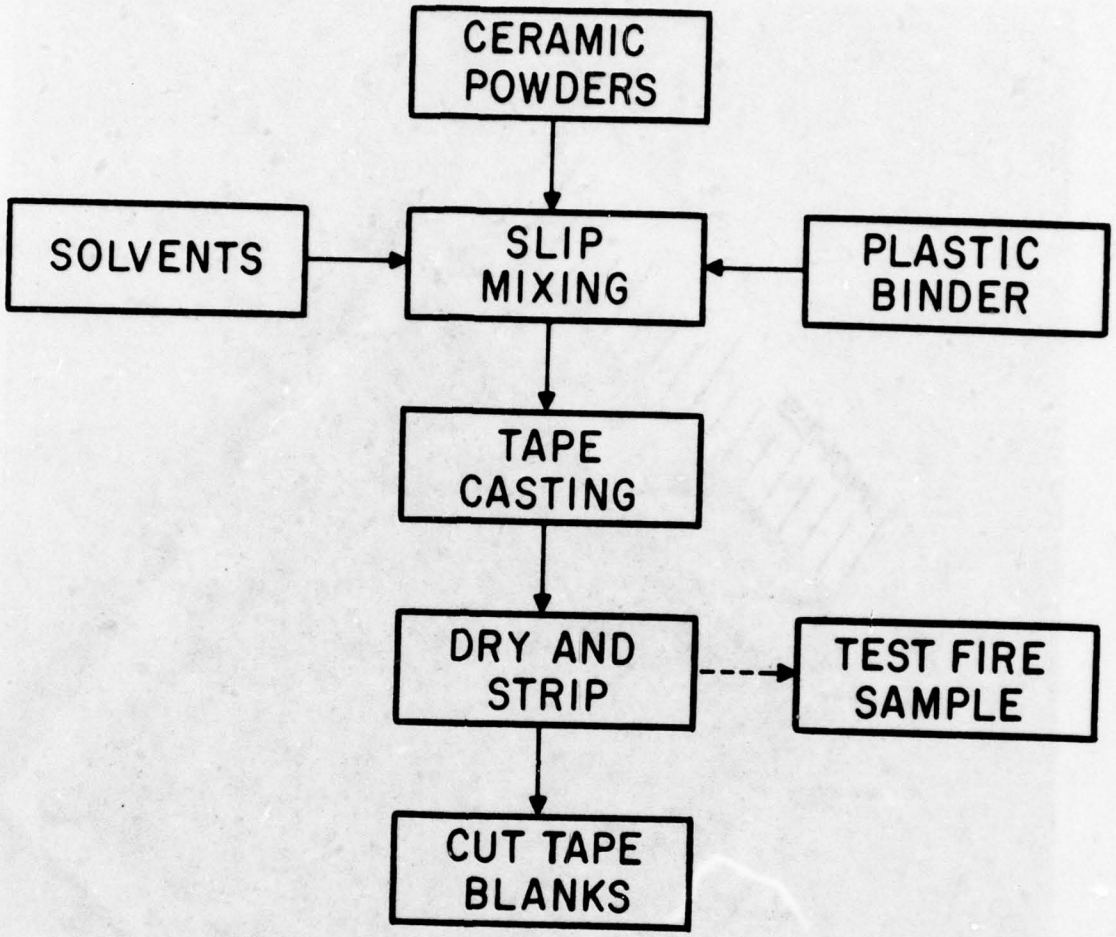


Figure 7. Green-Tape Preparation.

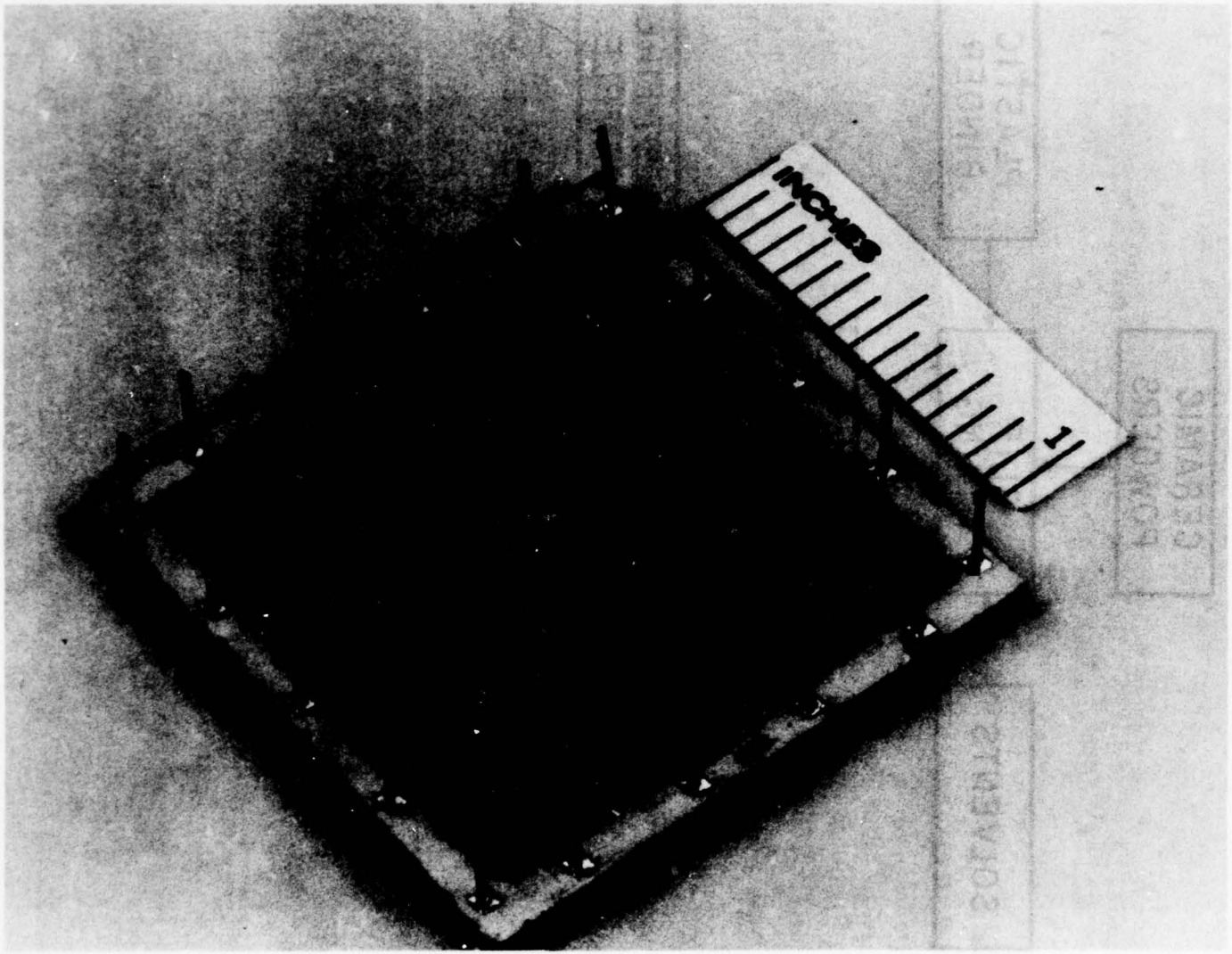


Figure 8. A 1.4-Inch-Square Multilayer Ceramic Substrate Assembly Containing 100 Flip-Chip Integrated Circuits.

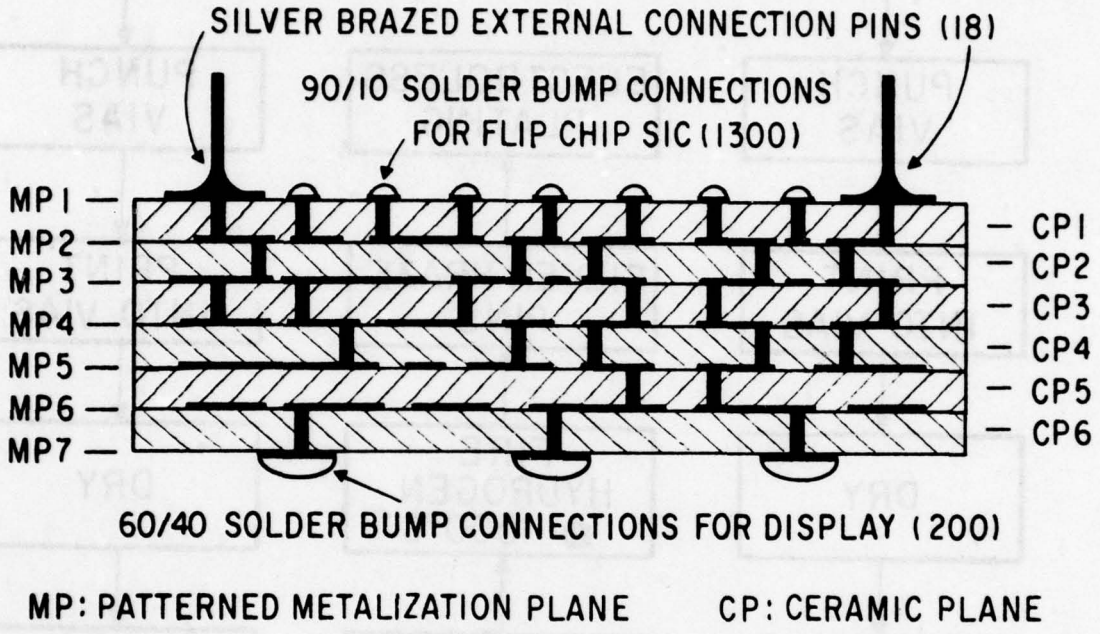


Figure 9. Schematic Cross Section Representation of the Multilayer Ceramic Substrate of Figure 8.

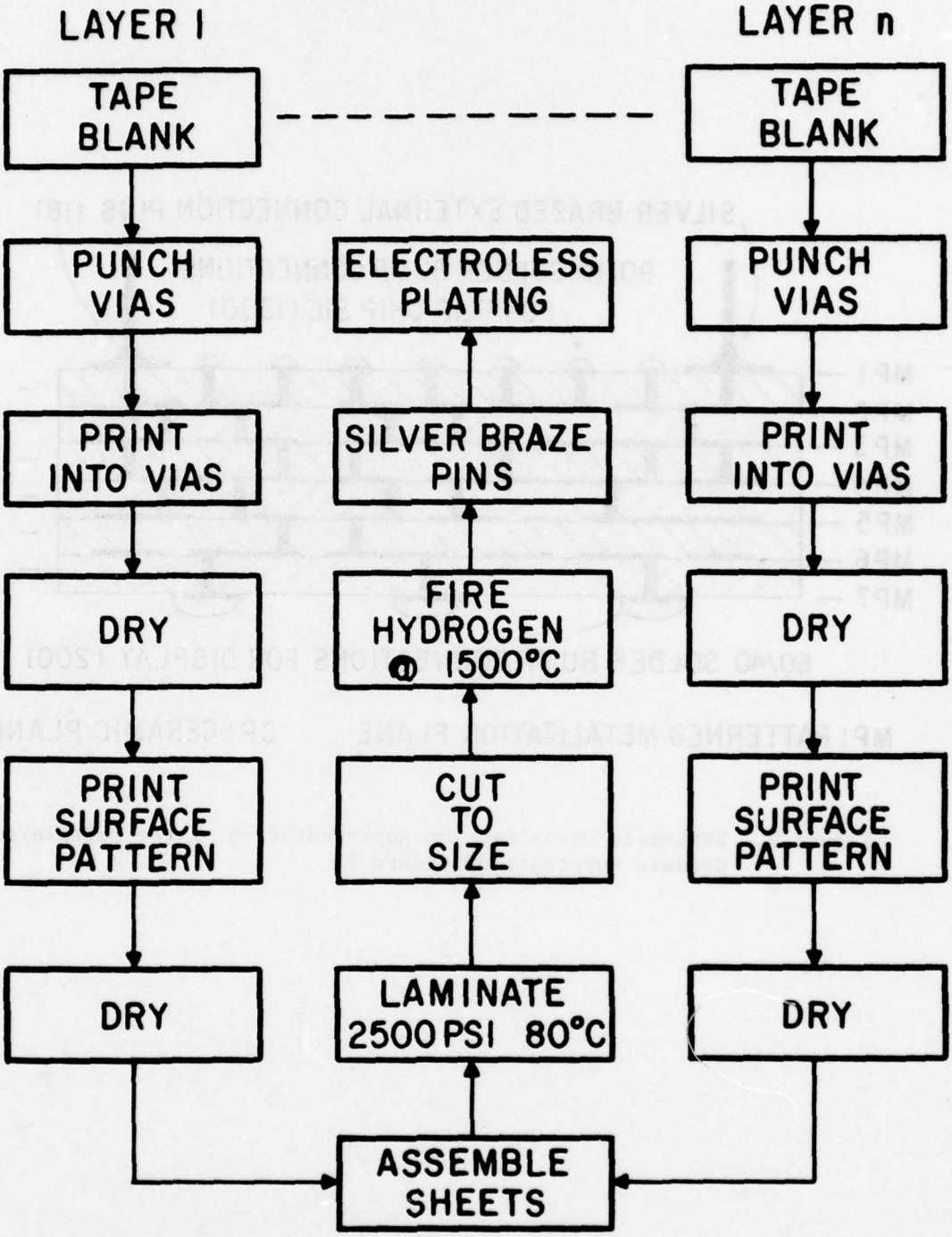
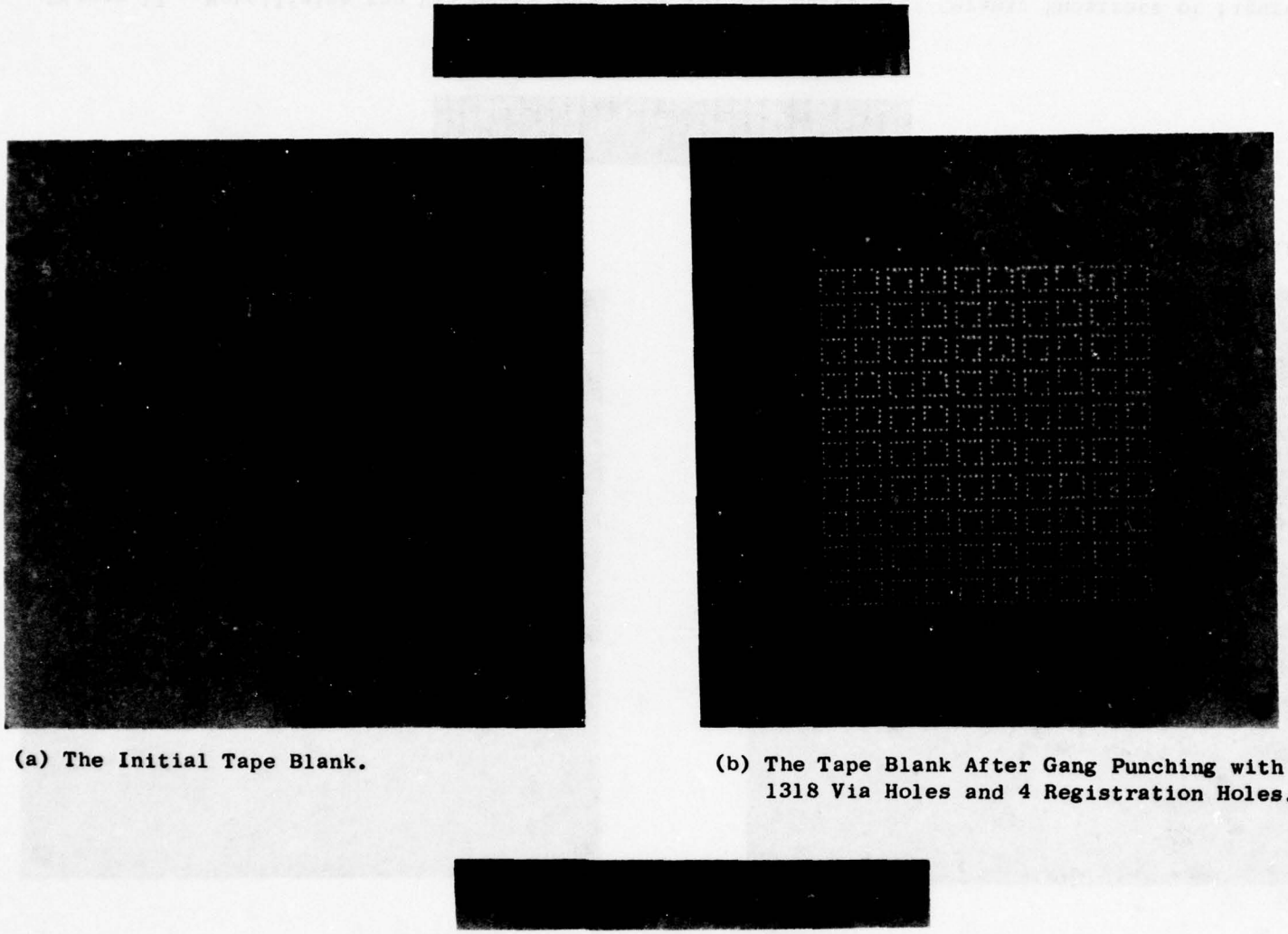


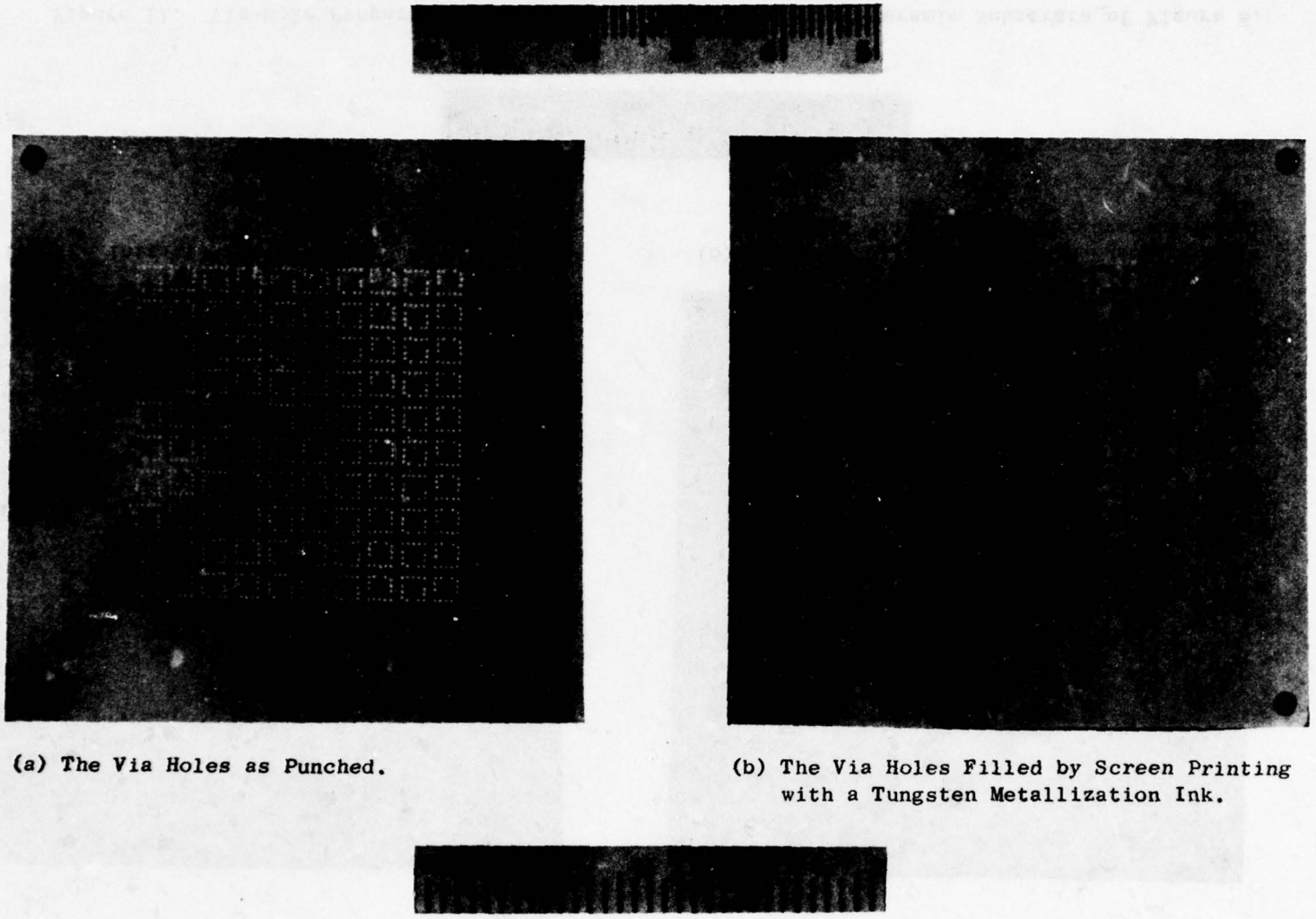
Figure 10. Multilayer Ceramic Substrate Process Sequence.



(a) The Initial Tape Blank.

(b) The Tape Blank After Gang Punching with 1318 Via Holes and 4 Registration Holes.

Figure 11. Via Hole Preparation in a Tape for the Multilayer Ceramic Substrate of Figure 8.



(a) The Via Holes as Punched.

(b) The Via Holes Filled by Screen Printing with a Tungsten Metallization Ink.

Figure 12. Metallizing the Via Holes in a Tape for the Multilayer Ceramic Substrate of Figure 8.

from the surface pattern, through the via, to the back side of the tape. This sequence is repeated for each of the required tape layers. Figure 13 shows the six completely metallized tape sheets required for the example and the finished fired substrate.

The series of six tape sheets then is stacked, one upon another, in register on a fixture containing four alignment pins - one for each corner alignment hole in the tapes. The stacked tapes then are laminated together under high pressure and elevated temperature; the thermoplastic binder softens, causing the individual sheets to fuse together inseparably. The laminate then is cut such that the firing shrinkage will produce the desired final size. The laminate then is fired at 1500° C in a hydrogen atmosphere to form the final monolithic ceramic interconnection structure.

After firing, the structure receives some additional operations. Input/output connections, such as pins or lead frames, are brazed on at high temperatures using alloy preforms and carbon fixtures. Plating, either electro or electroless, is applied to the tungsten metallization to improve its suitability to common assembly operations such as soldering.

Multilayer monolithic ceramic structures have a number of properties which recommend the technology for reliable hybrid assemblies. There is a very close match in thermal expansion between the two materials of construction: 6 μin/in./° C for alumina and 4 μin./in./° C for the tungsten metallization. Thus, temperature-induced internal stress is minimized, even over wide temperature excursions. The technology offers the ability to accommodate many layers of internal or buried conductor patterns. The thickness of the tape layers can be varied over a moderately broad range instead of the usual 0.010-inch thickness. Thick tapes - 0.025 inch - can be used to minimize parasitic capacitive coupling where required in fast logic circuits. Thin tapes - to 0.005 inch - can be used to increase capacitive coupling such as for bypassing power distribution conductors to ground planes. Small diameter via holes allow the use of high density conductor patterns. Details, such as sealing rims and recesses for silicon devices, can be integrated into the monolithic structure with ease to form a sealed package. The multilayer technology offers a wide range of design parameters, as shown in Table 4 (Reference 2).

The multilayer technology is not without some disadvantage, however. Gang punching of the via holes, necessary to maintain satisfactory registration among the layers, requires relatively complex tooling which is somewhat costly and time consuming to generate. The technology becomes expensive where the fixed tooling charges must be amortized over only a small number of piece parts. Tooling lead times are longer than for thin or thick film technologies and more expensive. Design changes which reflect into tooling changes are more difficult to implement.

Incorporating resistors into multilayer structures is more difficult than in normal thin or thick film technology. Thin film resistor depositions could be implemented on a multilayer structure if the surface were ground

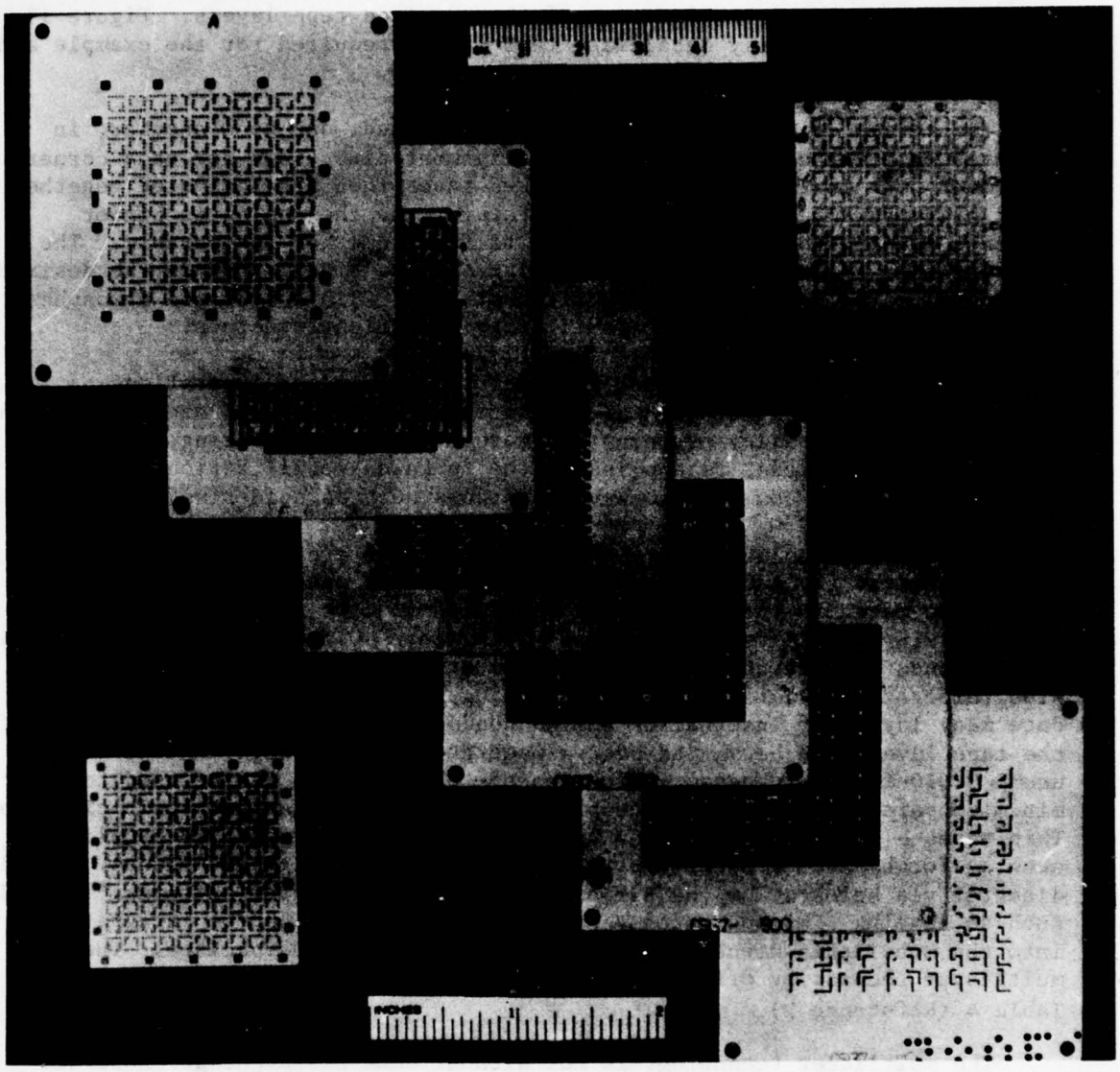


Figure 13. The Set of Six Green Tapes Required for the Multilayer Ceramic Substrate of Figure 8. (The As-Fired Substrate is Lower Left. The Finished Substrate is Upper Right.)

Table 4. Design Parameters for the Multilayer Ceramic Process (Ceramic Systems).

Parameter	Routine	Special
Conductor Width and Space, inch		
Surface	0.010	0.005
Internal	0.010	0.007
Via Holes, inch		
Diameter	0.008	0.005
Spacing	0.030	0.020
Dielectric Planes		
Number of Layers	2 - 10	20
Thickness, inch	0.010-0.015	0.005-0.025
Conductor Resistance, Ω/□		
Surface	0.010	0.005
Internal	0.015	0.010
Substrate Size, inches		
Maximum	2 × 2	4 × 4

and polished, but this would add substantially to the cost. Air-fired thick film resistor materials cannot be used with multilayer structures because the required air firing would damage or destroy the refractory tungsten metallization.

There appear to be two solutions to the resistor problem with multilayer ceramic structures, one proven and one potential. Chip resistors, either thin or thick film, can be used with ceramic multilayers as discrete attached components. Resistor networks, especially thin film on silicon, can be treated in a manner similar to integrated circuits for assembly onto ceramic multilayers and, thus, provide precision with high stability. The potential solution to adding thick film resistors lies in the newly emerging materials systems for firing in a protective nitrogen atmosphere. These are in development now by a few thick film materials suppliers for use with copper thick film conductors. However, this approach to adding thick film resistors to multilayer ceramics has not yet been reduced to practice.

b. Summary

Thin film provides the highest resolution and functional density of the current hybrid substrate technologies. It also provides the highest performance capabilities in resistor technology (precision, aging, matching, and temperature stability). It is seriously deficient in practical, useful dielectric materials. Simple crossovers require complex processing, and the technology has no capability for complex interconnection arrays containing multiple conductor layers. Therefore thin film was of no value to this advanced hybrid packaging.

Thick film can provide adequately good resistors of satisfactory performance. It has adequately good resolution capability and moderately high functional density. A variety of good dielectric materials is available, all with good electrical properties. Thick film has good multilayer capability and is widely used and accepted for the purpose. As many as six layers of conductors have been used in modest volume production. Although acceptable for many applications, thick film multilayer technology was ruled out for this hybrid program. The expansion mismatch between the dielectric and the substrate was counter to the goal of closely matched expansion throughout all materials of construction.

Multilayer ceramic has excellent multilayer capability, producing a rugged monolithic structure of materials closely matched expansion properties. It has good resolution capability and moderately high functional density. Relatively large assemblies have been demonstrated, up to 4 × 6 inches. It can be integrated easily into sealed package assemblies. Despite somewhat higher tooling cost and the longer lead time required, the multilayer ceramic technology was judged best suited for this advanced hybrid packaging. It is believed that the use of chip resistor networks is a satisfactory approach to providing resistors in multilayer structures.

These conclusions are summarized in Table 5.

Table 5. Summary of Significant Substrate Process Features.

Thin Film

+ Excellent resistors and conductors
+ High resolution and functional density
- No crossover or multilayer capability

Thick Film

+ Good resistors and conductors
+ Good resolution and functional density
+ Good multilayer capability
- Mismatched dielectric TCE

Multilayer Ceramic

+ Excellent multilayer capability
+ Rugged monolithic structure
+ Good resolution and functional density
+ Closely matched TCE, tungsten to alumina
- Resistors awkward
- Tooling and procurement time

5. Integrated Circuit Connection Technologies

a. General

A hybrid circuit is created upon the assembly of active semiconductor devices on a passive interconnection substrate. Bare semiconductor devices, devoid of their normal protective packages, are preferred in hybrid assemblies, thus conserving space. Typically, the active silicon device itself occupies less than 5% of the package area, often less than 2%. Mounting of the device chip to the substrate and connecting to it can be done by several established methods. The most common are flying leads, beam leads, flip-chips, and tape-automated bonding; each has its advantages and disadvantages.

The popular integrated circuit connection technologies are shown schematically in Figure 14. Die and wire bonding, which was prohibited for this program*, provides excellent heat transfer from the silicon device because the chip is bonded intimately to the substrate. Beam lead and flip-chip devices have poor heat transfer because the only significant cooling means is by conduction through the thermally high resistance beams or solder

*Recognizing the significant role played by the conventional flying-lead in hybrid reliability apportioning, one objective of the Hybrid Packaging Program was the selection and use of a more dependable connecting means.

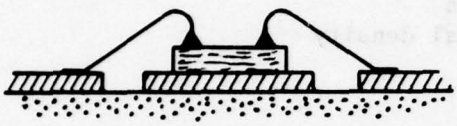
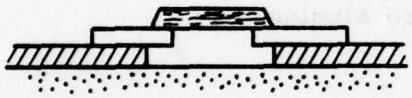
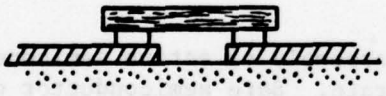
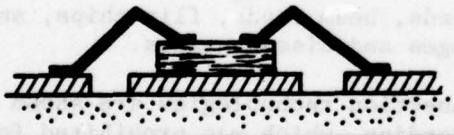
TYPE OF INTEGRATED CIRCUIT CONNECTION	DEVICE AVAILABILITY	HEAT TRANSFER CAPABILITIES Rth (J-s)
DIE AND WIRE BONDING 	GOOD	GOOD 2° to 10° C/W
BEAM LEAD 	POOR	POOR 50° to 100° C/W
FLIP CHIP 	POOR	MEDIUM POOR 25° to 75° C/W
TAB 	(GOOD)	GOOD 2° to 10° C/W

Figure 14. Schematic Representation and Comparison of Integrated Circuit Connection Technologies.

bumps. Device cooling by either of these two methods is inadequate for the projected needs. Tape-automated bonding (TAB) provides the same good heat sinking as does die and wire bonding. Thus TAB is a good connection candidate for hybrid packaging from thermal considerations.

b. Wire Bonding

The bulk of semiconductor devices produced for general use is designed for discrete packages and uses flying wire leads for connections within the package. Connecting pads of about 0.004 inch on centers as close as 0.006 inch accommodate 0.001 inch-diameter lead wires. Many hybrid circuit manufacturers use these conventional chips by proliferating the use of flying leads within the hybrid. In so doing, a vast selection of device types is available for hybrid needs - the same as is available in packaged form. Wire bonding has several disadvantages in hybrids. Having a high labor content, wire-bonded hybrids are more expensive and difficult to assembly. Yield and reliability suffer as the number of wire bonds increases. In-process repair requiring chip replacement is slow, difficult, and expensive and introduces the risk of destroying adjacent, otherwise good chips.

A serious constraint faced in hybrid applications is the inability to perform a realistic operational test upon a conventional chip prior to assembly in a hybrid. It is never known prior to electrical operation of the finished hybrid assembly, whether the semiconductor chips will function properly. For this reason, complex hybrids containing many wire-bonded devices have low yield as assembled and often require numerous repair cycles. Also, it is extremely difficult to temperature test or burn-in conventional chips prior to assembly.

c. Beam Leads

Many concepts have emerged for replacing flying leads, but, as yet, none of these have received widespread acceptance by the hybrid circuit industry as a whole. One is the beam lead. By special design and processing, a device chip is produced to include tiny integral gold ribbons extending slightly beyond the edge of the device, along its four sides. The cantilevered-beam-like ribbons are typically 0.004-inch-wide and long, 0.0005-inch-thick, and are on 0.010-inch centers. The beam lead chip is attached, face down, to the hybrid by its beams in a gang bonding operation. Planarity requirements for the beam bonding sites are stringent and are best satisfied by thin film interconnections. Beam lead devices are also used with thick film, but with difficulty. Gold substrate metallization is required for beam lead bonding, adding to the cost of such hybrids. Repair of a beam lead hybrid is very difficult.

Beam lead devices have a proven reliability greater than that of wire-bonded ones but are costly. Therefore, they have been used primarily in those applications where the need for high reliability was a dominant consideration and cost less important. Beam lead devices are difficult to handle because the beams are fragile. The major problem in attempting to

use beam lead devices is their lack of availability to the typical hybrid manufacturer, a problem also shared by flip-chip devices. This dominant consideration is discussed later.

d. Flip Chip

A very different approach to device assembly in hybrids is the flip-chip concept. Specially designed silicon chips are provided with hemispherical "feet" of solder bumps as connection points, which, later, also serve to attach the chip to its mounting substrate. The bumps are commonly 0.006-inch in diameter, 0.004-inch high, and are on 0.015-inch centers. A matching "footprint" of connecting pads is provided on the interconnecting substrate and coated with solder. The chip is placed in alignment with the footprint, bumps down. A simple heating operation causes the solders to melt and flow together, simultaneously adjusting the chip to its correct location while joining it to the mounting pads.

The flip-chip concept has the unique ability to assemble a multiplicity of chips on a substrate simultaneously with one simple heating operation. Other components, like chip capacitors, also can be attached during the same operation. This procedure results in very low assembly cost and high productivity. Flip-chip assemblies are easily repairable by locally heating the repair site to replace a chip without disturbing its neighbors. The flip chip is an ideal match with the solder-oriented thick film technology. However, for the typical hybrid manufacturer, flip chip shares the lack-of-device-availability problem in common with beam lead.

If the necessary devices became available immediately, both the beam lead and flip-chip technology would become more useful to the hybrid manufacturer. No significant variety of devices is available now in the open market place. A few major hybrid manufacturers, with wisdom, conviction, and adequate resources, have chosen one of these technologies and forced it to serve their needs realistically. Western Electric and Raytheon have been brilliantly successful with beam leads, while International Business Machines and Delco have shown similar success with flip chips. These users have succeeded only because each had a captive silicon processing capability responsive to their own needs. This luxury is not available to the ordinary hybrid fabricator.

e. Tape-Automated Bonding

The relatively new cinema tape assembly technology is now beginning to have a major impact within the semiconductor industry. Many silicon suppliers now believe that tape-automated bonding, which is an outgrowth of GE's Minimod concept will be the best method of replacing wire bonding in their products. In fact, the originators of beam leads and flip chips are evaluating the technology. Tape bonding already has gained wide acceptance among the major IC suppliers, and many now have tape-oriented processes in production for their standard packages ICs. Tape bonding also has aroused new interest in the hybrid industry.

Tape-automated bonding employs a cinema-film-like tape as a hands-off carrier for individual ICs that is used from wafer through realistic dynamic functional testing to final assembly. A sturdy, etched-copper, finger-like pattern of connections converge inward, projecting over a precisely punched area in the tape. The inner-end geometry of the leads matches that of the IC connection pads. Enlarged outer lead areas, attached to the tape, provide connection pads for reliable, in-process, dynamic probe testing of the IC while carried by the tape. Sprocket holes near both edges are precisely registered to the central hole pattern and "remember" the exact IC location while transporting the carrier film through the various processes.

Assembly machines, ranging from simple manual through fully automatic operation, have been developed to handle all aspects of the tape bonding process, from tape preparation through final IC placement. Individual ICs are attached to leads in precise registration to the sprocket holes. Thereafter many ICs are simultaneously handled as a single reel of tape. At assembly, individual ICs with leads attached are released from the tape and joined to a substrate while preserving the original accuracy of location. A high degree of automation is practical with tape-automated bonding, thus greatly reducing assembly cost and improving yield.

Tape bonding requires the device to have bumped lead bonding pads just like the flip chip. Metallurgies have been established for a choice of thermocompression, gold-tin eutectic or solder-reflow lead attachment to the IC. However, unlike flip chip, a specially designed connecting pad geometry is not required. Any existing IC, even those designed for wire bonding, can be accommodated by adding the bumps and providing an easily designed lead pattern. Thus tape bonding makes all existing and future ICs available to the hybrid manufacturer without his having to resort to wire bonding.

The growing acceptance and in-house use of tape bonding by major semiconductor manufacters will greatly benefit hybrid houses. Some vendors now offer their standard products on reels of tape. Others are supplying prepared wafers, ready for tape mounting by the user. Conceivably, those semiconductor houses employing a tape bonding process would be prime candidates to supply custom ICs, either as wafers ready for tape mounting or individual devices already mounted on reels of tape.

f. Summary

Because one of the major program goals was to develop a better connection technology, the die and wire bonding technique was eliminated from this packaging program. Beam lead and flip-chip technologies were found unsuitable because of the total unavailability of the necessary devices and the poor heat transfer inherent in both approaches.

Tape-automated bonding has excellent prospects for hybrids. It promises to ease the device availability dilemma by accommodating existing devices. Heat transfer is good. TAB offers the potential of low cost assembly with its capability for mechanization and automation. The tape technology permits

realistic performance testing of devices while they are still aboard the tape. Even burn-in of tape-mounted devices seems feasible. Inclusion of these operations prior to assembly should result in high assembly yields and greatly improved operating reliability even in complex, multiple-chip hybrids. Operational reliability should be further enhanced by having connections which are made with sturdy, beam-like leads. For theses reasons, TAB was chosen as the integrated circuit connection technology for this hybrid packaging program.

A comparison among the connection technologies is given in Table 6.

6. The Tape-Automated Bonding (TAB) Process

a. General

The concept of using a cinema film-like carrier for handling semiconductor devices had its origin at General Electric in the late 1960's. General Electric developed the process into its Minimod line products offered in the early 1970's. Shortly thereafter, all film carrier activity ceased within General Electric. In recent years there has been renewed interest, particularly by semiconductor suppliers who have adopted the process for their manufacturing needs. A few hybrid circuit processors also have been attracted to the process. Most notable of these are CII-Honeywell Bull and Honeywell Information Systems, each of whom has greatly advanced the process to serve their hybrid needs. Other users of tape bonding in experimental-to-production applications are shown in Table 7. The name "Tape-Automated Bonding" (TAB) originated with CII-Honeywell Bull to describe their own process but is now often used for the tape carrier process in general (Reference 3).

The key operations of the TAB process are shown schematically in Figure 15. The initial process components are a prepared silicon wafer on a carrier plate, A, and a reel of carrier tape, B. The wafer has been bumped and sawn, but the individual silicon devices remain fixed on the carrier plate in their original wafer locations. The tape contains a repeating pattern of sprocket holes, a central window, and a group of formed leads converging into the window. The inner ends of a lead pattern are designed to match the connection pad locations of an individual silicon chip.

The tape and wafer merge in a process called "inner lead bonding," C. This operation simultaneously transfers an individual chip to the tape while connecting it to the leads of a frame of tape. Then, an optional electrical operational test, D, can be performed on the tape-mounted chips. Individual chips then are freed from the tape and assembled, in the "outer lead bonding" operation, attaching to either a lead frame, E, or to a hybrid, F. These key operations are all amenable to mechanization or automation. There is no need to manually handle individual chips from the original wafer to the final assembly.

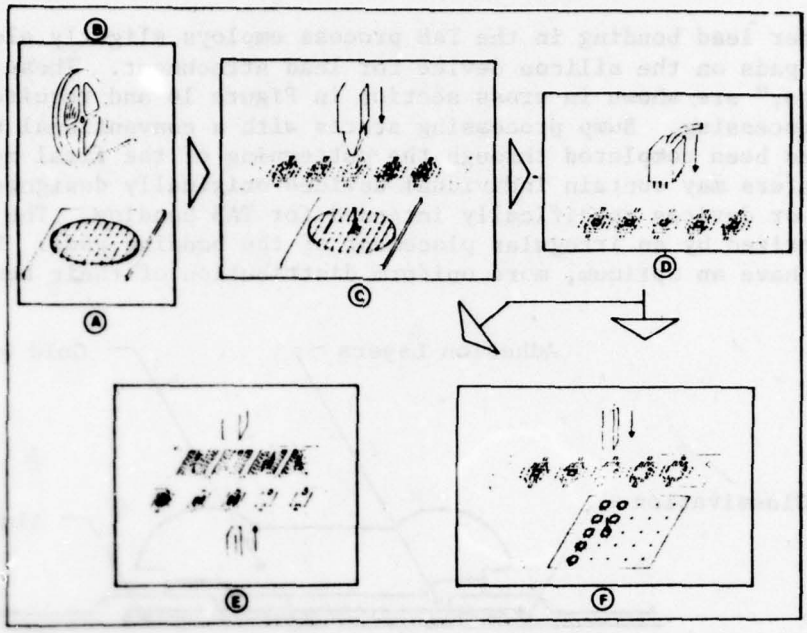
Table 6. A Comparison of Integrated Circuit Connection Technology Features.

Die & Wire Bonding	Beam Leads
+ Broad Device Variety	+ Mature Technology
+ Layout Flexibility	+ Established Processing
+ Good Heat Transfer	+ Documented Reliability
+ Eutectic, Solder, or Adhesive Mounting	+ Demonstrated Applications
- High Labor Content	- Limited Acceptance
- Reduced Assembly Yield	- Inadequate Device Variety
- Intermetallic Plagues	- Poor Heat Transfer
- Individual Chip Handling	- Individual Chip Handling
- High Operator Error Risk	- Preassembly Test Difficult
- Difficult to Repair	- High Device Cost
	- Difficult to Repair
Flip Chips	**Tape-Automated Bonding**
+ Can be Mechanized	+ Accomodates Existing Devices
+ Self-Aligning	+ Can be Fully Automated
+ Simultaneous Mass Assembly	+ No Manual Device Handling
+ Can be Pretested	+ Preassembly Dynamic Test
+ Easiest to Repair	+ Tape Design Versatility
- Limited Acceptance	+ Gang Bonding of Connections
- Inadequate Device Availability	+ Wafer-to-Assembly Registration
- Poor Heat Transfer	+ Excellent Mechanical Strength
- Individual Chip Handling	+ Excellent Heat Transfer
- Hidden Connections	+ Low Assembly Cost
	+ Improved Reliability
	- Emerging Process

Table 7. Tape Bonding Users (Courtesy of International Micro Industries).

Semiconductor Industry		
Domestic:		
Fairchild	Motorola	Signetics
Hughes	National	TI
ITT	RCA	Westinghouse
Foreign:		
Phillips	Fujitsu	NEC
Siemens	Hitachi	Sharp
Telefunken	Matsushita	Toshiba
	Mitsubishi	

Hybrid Industry		
Domestic:		
Burroughs	Hughes	Motorola
Hewlett Packard	IBM	TI
Honeywell	ITT	Western Electric
		Westinghouse
Foreign:		
Honeywell Bull	Cannon	OKI
Saab Scania	Citizen	Sanken
Siemens	Copal	Sanyo
Telefunken	Datsun	Seiko
Thompson CFS	Fujitsu	Sharp
	Hitachi	Sony
	Matsushita	Toshiba
	Mitsubishi	Toyota
		Yashika



(A) Wafer preparation

(B) Tape preparation

(C) Inner lead bonding

(D) Electrical test

(E) Outer lead bonding to lead frames

(F) Outer lead bonding to hybrid substrates

Figure 15. Key Steps in the Tape-Automated Bonding (TAB) Process.

b. Wafer Preparation

Inner lead bonding in the TAB process employs slightly elevated connecting pads on the silicon device for lead attachment. These raised pads, or "bumps," are shown in cross section in Figure 16 and require additional wafer processing. Bump processing starts with a conventional silicon wafer, which has been completed through the patterning of the final metallization. These wafers may contain individual devices originally designed for wire bonding or devices specifically intended for TAB bonding. The former are characterized by an irregular placement of the bonding pads. Devices designed for TAB have an optimum, more uniform distribution of their bonding pads.

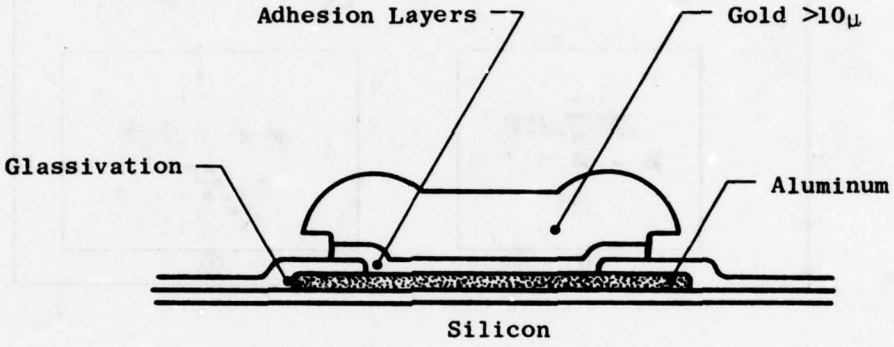


Figure 16. Schematic Cross Section of a Gold Bump.

A layer of passivation glass is applied over the surface of the wafer. Openings are made in the passivation over the original bonding pads, slightly smaller than the pads themselves. A thin layer of one or more metals then is applied over the passivation layer and through the openings, onto the exposed aluminum pad areas. Metals such as chromium, nickel, tantalum, titanium, and tungsten have been used. The function of this intermediate metallic barrier layer is threefold: (1) it provides good adhesion to the aluminum beneath; (2) it also protects the active aluminum from contamination and prevents it from reacting metallurgically with other metals to be applied above the barrier layer; and (3) later, the barrier layer also will support the necessary electrical current for electroplating a thick bump.

The barrier layer is covered with a photoresist coating. Openings then are made in the photoresist over the bonding pads - slightly larger than the windows in the passivation but slightly smaller than the original bonding pad size. The metallic barrier layer now is exposed at the bonding pads, but elsewhere this layer is covered with the electrically insulating photoresist. Now, bumps are built over the bonding pads by electroplating to a height of 0.0005 to 0.001-inch (the usual materials being either gold or copper). Removal of the photoresist exposes the barrier layer which is removed by

chemical etching except where it is protected beneath the electroplated bumps over the bonding pads.

Then the bumped wafer is attached to a carrier plate with a thermoplastic adhesive such as a wax. Next, the wafer is diamond sawed to separate it into a matrix of individual silicon devices. These remain fixed in their original wafer positions, held in place by the adhesive during the sawing. A prepared wafer on its carrier is shown in Figure 17. Figure 18 shows part of a wafer matrix. The raised bumps are visible as well as the saw kerf separating the individual chips. By using a thick laminated film photoresist, the bump height can be increased while maintaining the well-defined shape. Bumps 0.0015 inch tall, made with film resist, are shown in Figure 19.

c. Conventional Tape Preparation

The tape serves two primary functions in the TAB process. It carries the individual silicon chips from wafer through final assembly. It also provides sturdy connecting leads from the chip to the assembly. A variety of tape widths and constructions have satisfied the primary requirements for various applications. Widths of 8, 11, 16, 35, and 70 mm have been used in one-, two- and three-layer construction. A patterned metal-foil ribbon constitutes a one-layer tape. A two-layer tape adds a skeletal polyimide pattern to the one-layer tape. Neither the one- nor the two-layer tape is of interest for hybrid applications because such construction denies the opportunity of testing chips on such tapes.

Tapes for hybrid circuit applications usually have three-layer construction: a supporting plastic film 0.003-inch or 0.005-inch thick, an adhesive film, and a metal foil (normally 0.0013-inch copper). For superior dimensional stability and inertness a polyimide film is preferred, especially when a portion of the film remains with the product, as happens in TAB processing for packaging discrete semiconductor devices. Stabilized polyester film also has been used successfully where the film is subjected to process temperatures that are only mildly elevated.

The preparation of TAB tapes is illustrated in Figure 20. In this case, a 35-mm-wide polyimide film, an adhesive film, and a polyethylene film protecting the adhesive surface are sandwiched together. The sandwich is punched periodically with a single frame of a repeating hole pattern. The pattern contains four sprocket holes, two central windows, and two sets of cutout brackets, all precisely registered to each other within the pattern. Two strips of copper foil are laminated centrally between the rows of sprocket holes and are adhered to the polyimide film by the thermosetting film adhesive layer. The copper strips are coated with photoresist, and then this resist is exposed with the desired lead pattern. The exposure is repeated frame-by-frame with the pattern master registered to the sprocket holes of the frame being exposed. Thus, each group of leads is always precisely located with respect to its own sprocket holes. After exposing and developing the photoresist, the copper is chemically etched. The undesired copper is removed leaving only the desired copper - the lead pattern. The copper then is tin

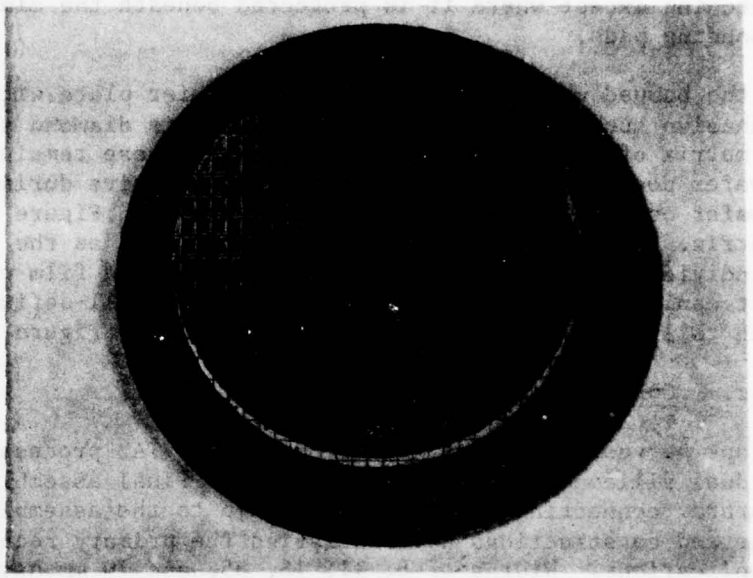


Figure 17. A Wafer Matrix of Integrated Circuits on a Carrier Plate. Shown are the Fairchild 93S16 Chips Used to Construct the Memory Module.

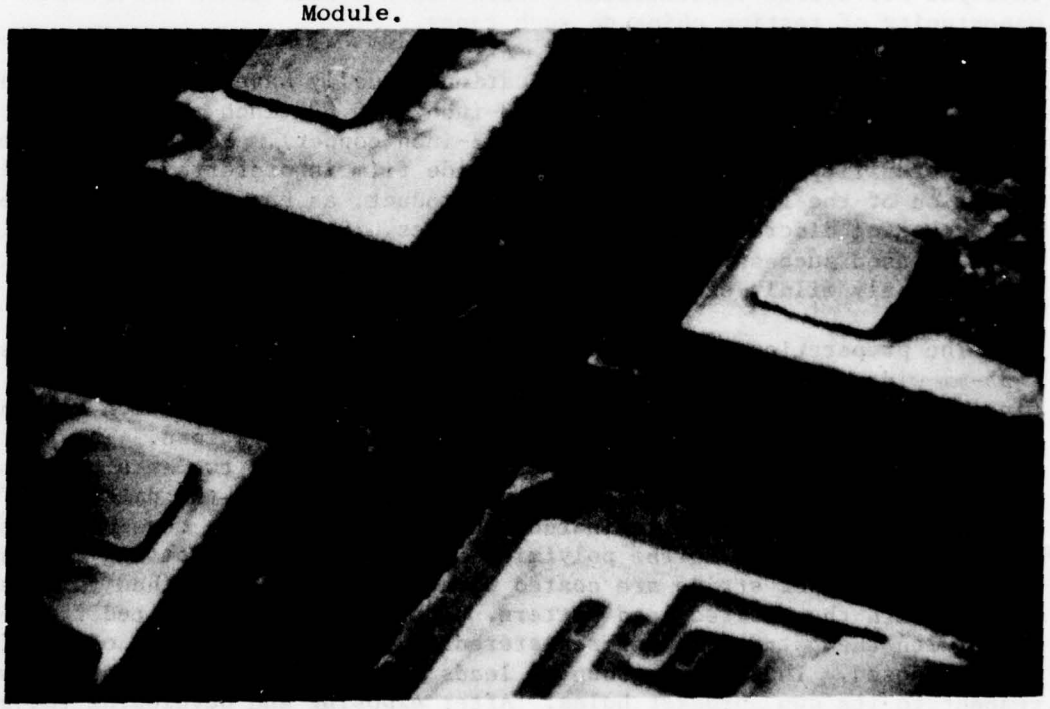


Figure 18. SEM View of Part of a Wafer Matrix Showing the Raised Gold Bumps and the Diamond-Saw Kerf.

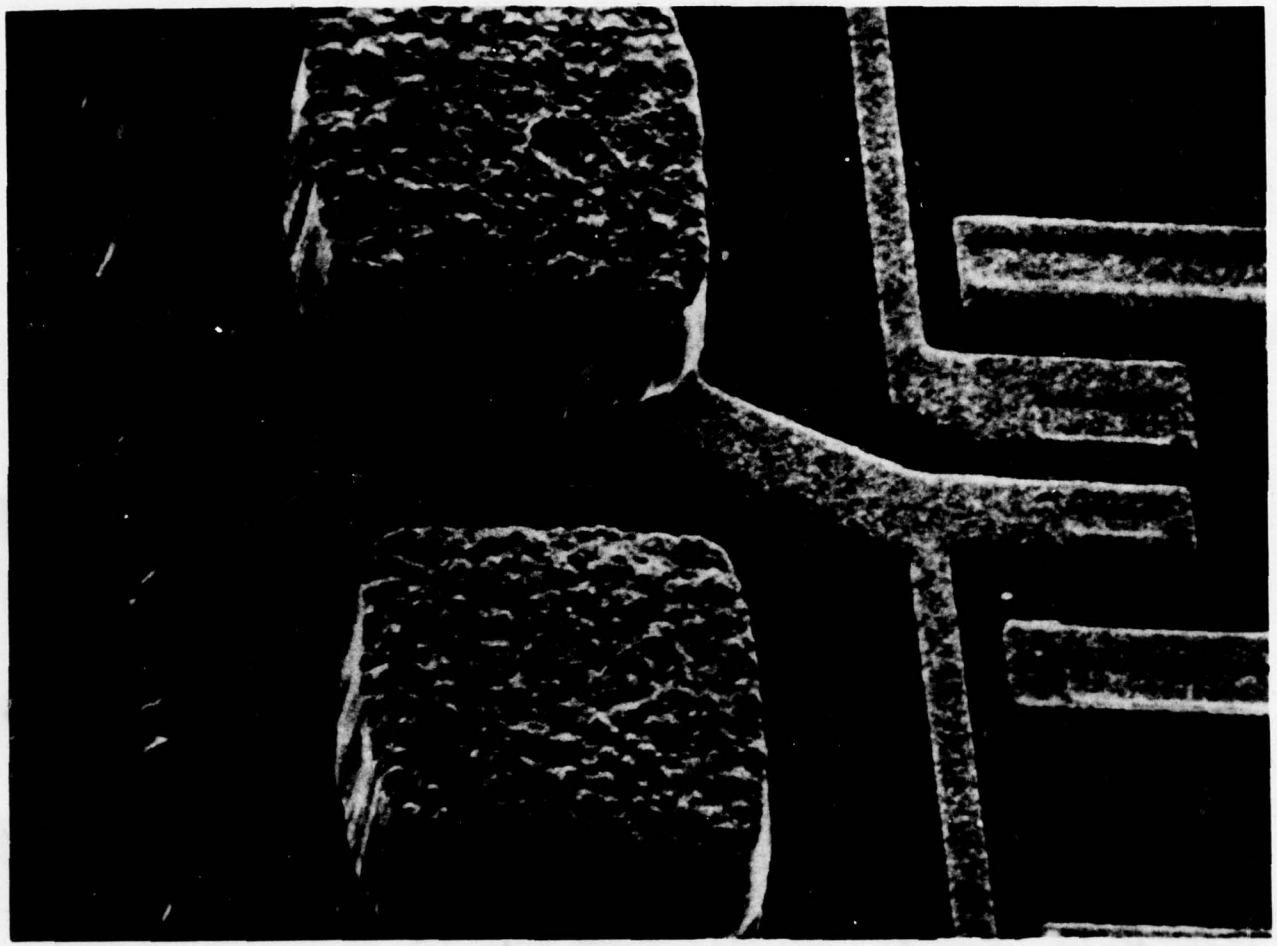
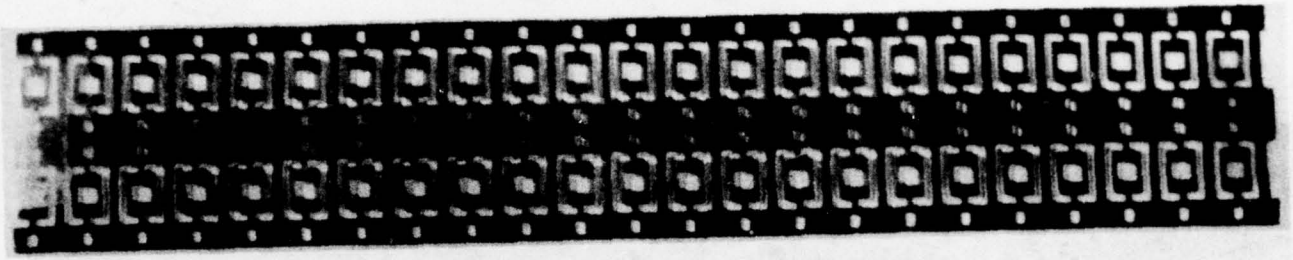
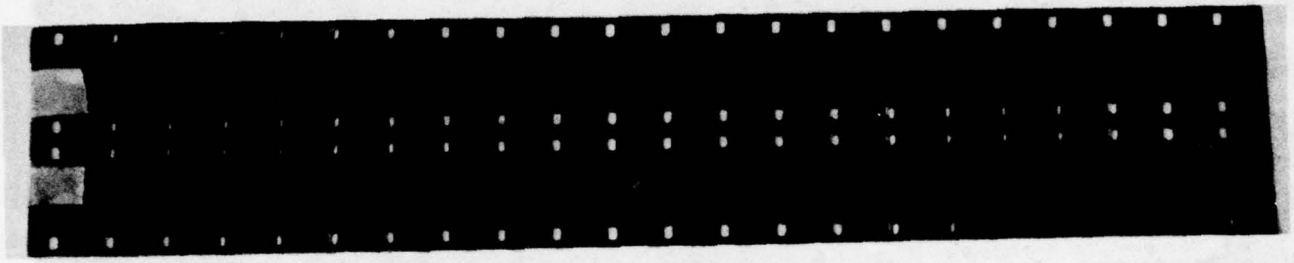


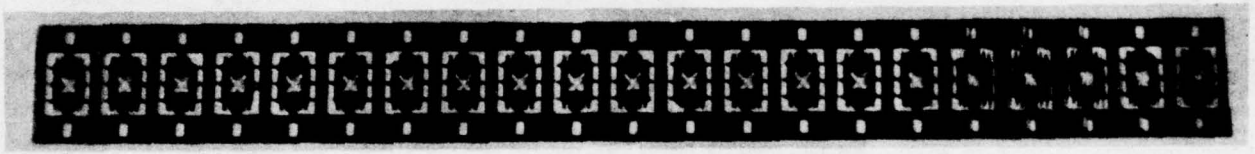
Figure 19. SEM View of Tall Gold Bumps Prepared with Film Photoresist.



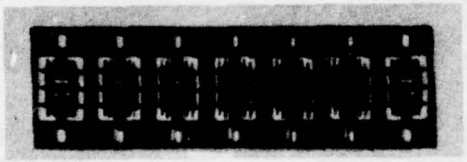
(a) Punched 35mm-wide Polyimide Film.



(b) Copper Strips Laminated to Film.



(c) Photoetched TAB Leads on Film Slit to 16mm Width.



(d) Integrated Circuit Chips Attached.

Figure 20. TAB Tape Preparation.

plated as discussed in Section II.d. The 35-mm tape is slit into two 16-mm tapes, each ready for inner lead bonding.

TAB tapes 35-mm wide (Figure 21) are more popular for hybrid circuit applications. The greater width accommodates larger semiconductor chips and allows the inclusion of the most important probe test pads used for testing chips while they are mounted on the tape. Figure 22 shows the finished leads.

Starting with this existing technology as background, the introduction of Kovar in place of copper was a major development performed in the Hybrid Packaging Program.

Kovar was used instead of copper because the thermal expansion properties of Kovar provide a close match to those of alumina. This is discussed in detail in subsequent Section III.3.

d. Bonding Technologies

Both inner lead and outer lead bonding can be accomplished by either thermocompression or fusion techniques. The choice depends upon the application, its requirements, and bonding equipment availability. Thermocompression bonds are formed between two metals by the application of heat and pressure. The pressure must be sufficiently high to cause the metals to cold-flow slightly. This flow distorts the mating surfaces exposing fresh, new uncontaminated areas which readily weld together at the elevated temperature. Thermocompression bonding of copper-to-copper at 600° C and gold-to-gold at 300° C produces connections.

Thermocompression bonding has disadvantages. A high force is required, sufficient to deform the materials to be joined. For successful gang bonding of inner or outer leads, the surfaces involved must be relatively flat or coplanar. If the bonding pressure is not distributed uniformly, it will be too low to create a satisfactory bond in some areas or so high that local damage results in other areas. Silicon device damage can result or substrates can be cracked by excessive local pressure. A thermocompression bond shows little visible evidence of the bond quality other than the deformation of the bonded members. However, when controlled carefully, thermocompression bonding has been very successful. It has the advantage of being unaffected by exposure to temperatures higher than that at which the bond was initially formed.

For copper-to-copper thermocompression bonding, the leads of a TAB tape can be unprotected copper, and the bumps on the silicon chip also would be copper. This combination would have a short useful storage life before the bare copper surfaces gathered sufficient oxide to inhibit satisfactory bonding. Sometimes a thin flash of gold is plated over the copper to preserve its bonding properties. For gold-to-gold bonding, a thicker plating of gold is placed on the copper leads and gold-bumped silicon chips are used.

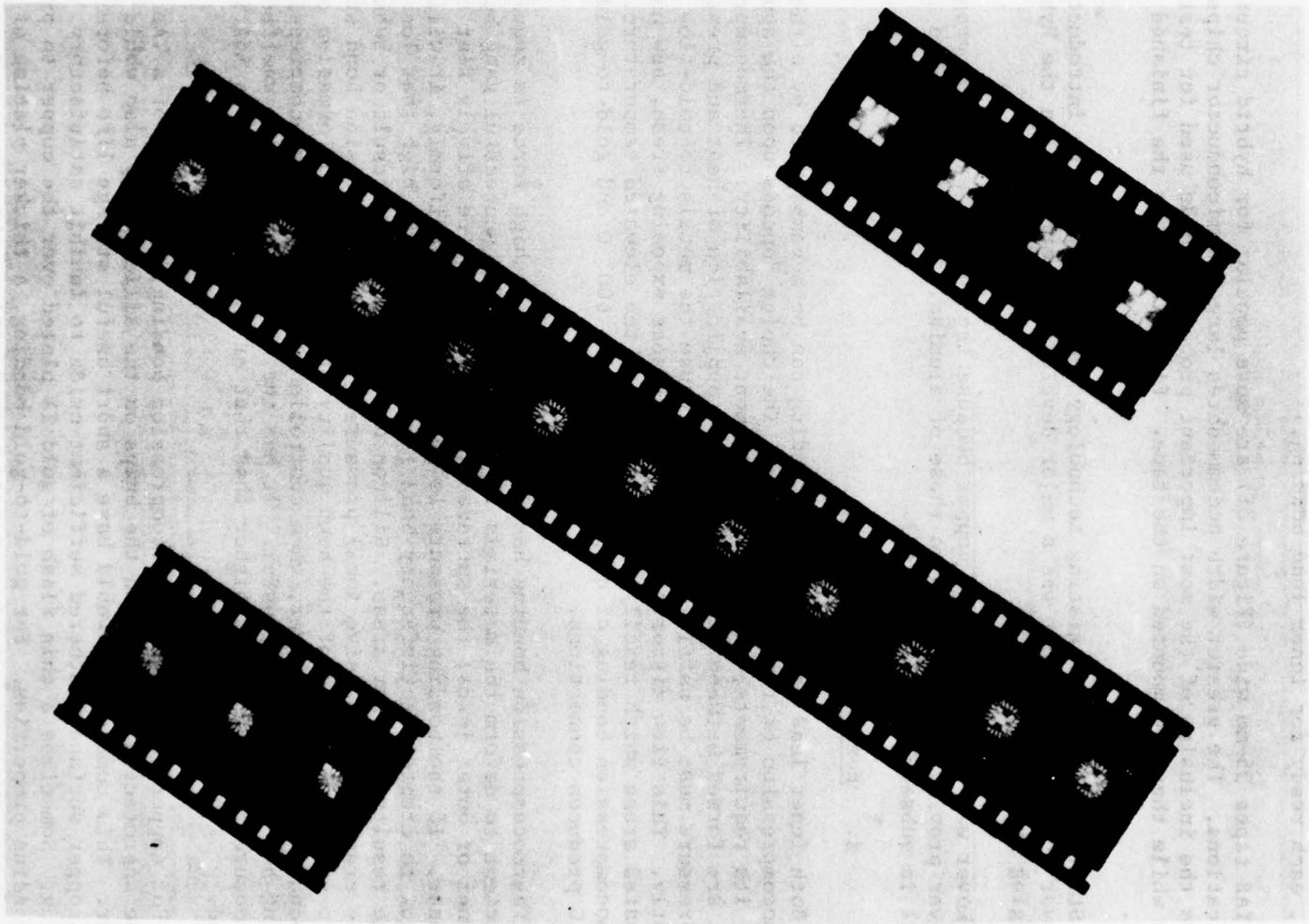


Figure 21. TAB Tapes for Hybrid Circuit Application. The 35mm Width Accomodates Pads for Electrical Testing of Chips on Tape.

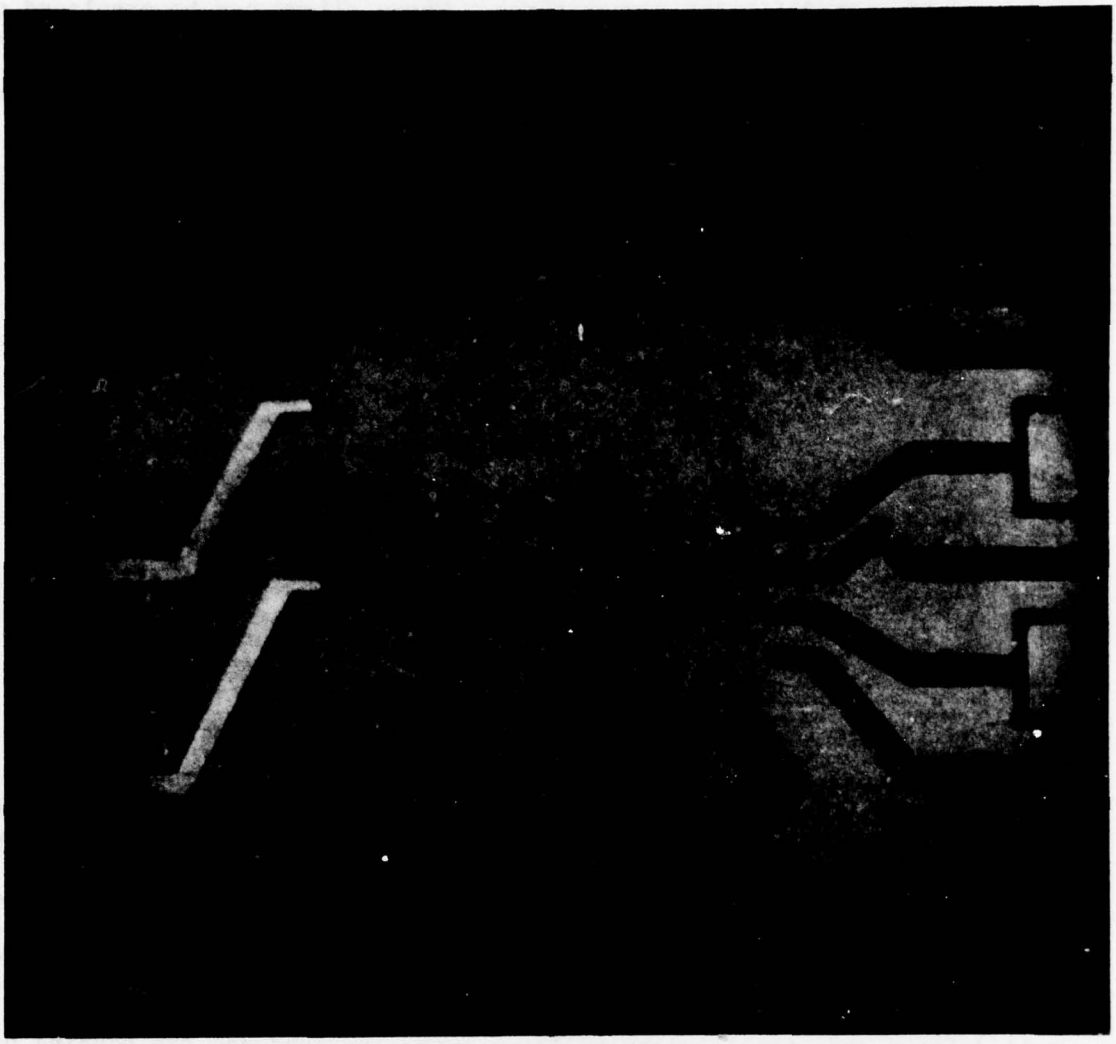


Figure 22. The Inner Lead Region of TAB Tape Leads. (Courtesy of CII Honeywell Bull.)

Fusion bonding can be performed with a variety of metals or alloys which melt and flow at different temperatures. These alloys can be preplaced or can be formed in situ. Table 8 shows some of the solder alloys that have been used, along with their melting temperatures. A thick layer of tin electroplated on the copper leads had been used to "solder" to copper bumps in production.

Table 8. Bonding Metallurgies Frequently Used in the Tab Process.

Thermocompression		
Copper-to-Copper		600° C
Gold-to-Gold		300° C
Solders		
Tin Lead	10:90	320° C
Gold Tin	80:20	280° C
Tin	100	240° C
Lead Indium	75:25	230° C
Lead Indium	50:50	215° C
Tin Lead	63:37	200° C

A particularly successful inner lead fusion bonding method employs in situ alloying. Electroless tin is plated onto the tape leads to a thickness of about 25 microinches. The tin-plated leads are brought into contact with gold bumps on a silicon chip beneath a pulse-heated tool. A brief pulse of heat is applied. This causes the tin to melt first and then rapidly alloy with the gold of the bump. Thus, in situ gold-tin alloy is formed, an alloy whose final composition can be closely controlled by the thickness of the tin plating and the temperature of the heating tool, resulting in the proportions of 80% gold, 20% tin. Such a bond has the distinct advantage of forming a well-defined and visible alloy fillet between the lead and the bonding pad. Thus, it is very easy to monitor the quality of the resulting inner lead bonds visually. Also, fusion bonding has the advantage of allowing graded-temperature assembly operations. The alloys can be selected so the next operation is performed at a temperature somewhat lower than the previous one, to avoid disturbing it. For example, inner lead bonds at 280° C with 80% gold/20% tin, die bonds at 230° C with 75% lead/25% indium, and outer lead bonds at 215° C with 50% lead/50% indium can be made.

e. Inner Lead Bonding

A silicon chip is attached to the leads of a TAB tape frame and simultaneously released from its carrier plate in the inner lead bonding operation. An inner lead bonding machine performs this operation either semiautomatically with manual guidance or fully automatically. Such equipment is well developed

and readily available. A representative manually assisted inner lead bonder used at General Electric's Corporate Research and Development Center is shown in Figure 23. The operator simply aligns a silicon chip to a reference graticule in the viewing microscope. Thereafter, the bonding of that chip is automatically performed by the bonder. More sophisticated equipment also is available which automatically bonds all chips from a whole wafer following an initial alignment of the wafer.

The manually assisted inner lead fusion bonding operation is illustrated in Figure 24. A chip, or die, is aligned visually beneath the inner ends of a group of leads (a). The die is viewed optically and aligned manually. As the bonding operation begins (b), the tape is positioned to bring the leads into contact with the bumps. The area is flooded with an inert cover gas to protect the die and leads. The bonding tool descends (c) pressing the leads against the pads. A pulsed electric current heats the tool, forming the bond between the leads and the bonding pads. The heat of bonding the leads also melts the adhesive beneath the die, releasing it from the carrier.

After completing the bond (d), the tool retracts. Then, either the tape track is raised or the die carrier is lowered, lifting the bonded die free from the melted adhesive. Finally, the tape is indexed to the right (e) to bring a new frame of tape leads into bonding position. The X-Y table bearing the die is indexed to the left to bring the next die into bonding position. A fully automatic inner lead bonder would index the die and repeat the inner lead bonding operation until the supply of die became exhausted.

A tape-mounted chip is shown in Figure 25. The inner lead bonding region is shown in Figure 26. Figure 27 shows scanning electron microscope views of inner lead bonds (a) and a well-defined fillet (b) formed by gold-tin fusion bonding.

f. Electrical Test of Devices

As hybrid assemblies grow in complexity, it becomes increasingly imperative that all the silicon devices operate properly after assembly. Otherwise, assembly yield can decrease to the extent where it becomes nearly impossible to produce an operating circuit without a prolonged series of repairs. Repeated repair of a hybrid assembly is undesirable. Often the act of repairing one area inflicts new damage to another area. Instead, it is better to strive toward the highest possible yield of an assembly the first time through.

The effect of individual silicon device yield and hybrid circuit complexity on assembly yield is shown in Figure 28. Wire-bonded hybrid assemblies have an average, first-time-through, individual chip yield of about 95%. This equates to an assembly yield of only 60% for a 10-chip assembly. One out of three assemblies will be inoperative upon completion. The use of a high temperature eutectic die attach can further reduce the individual wire-bonded chip yield to around 90%. Now two out of every three 10-chip assemblies will be inoperative upon completion. It has become virtually impractical to

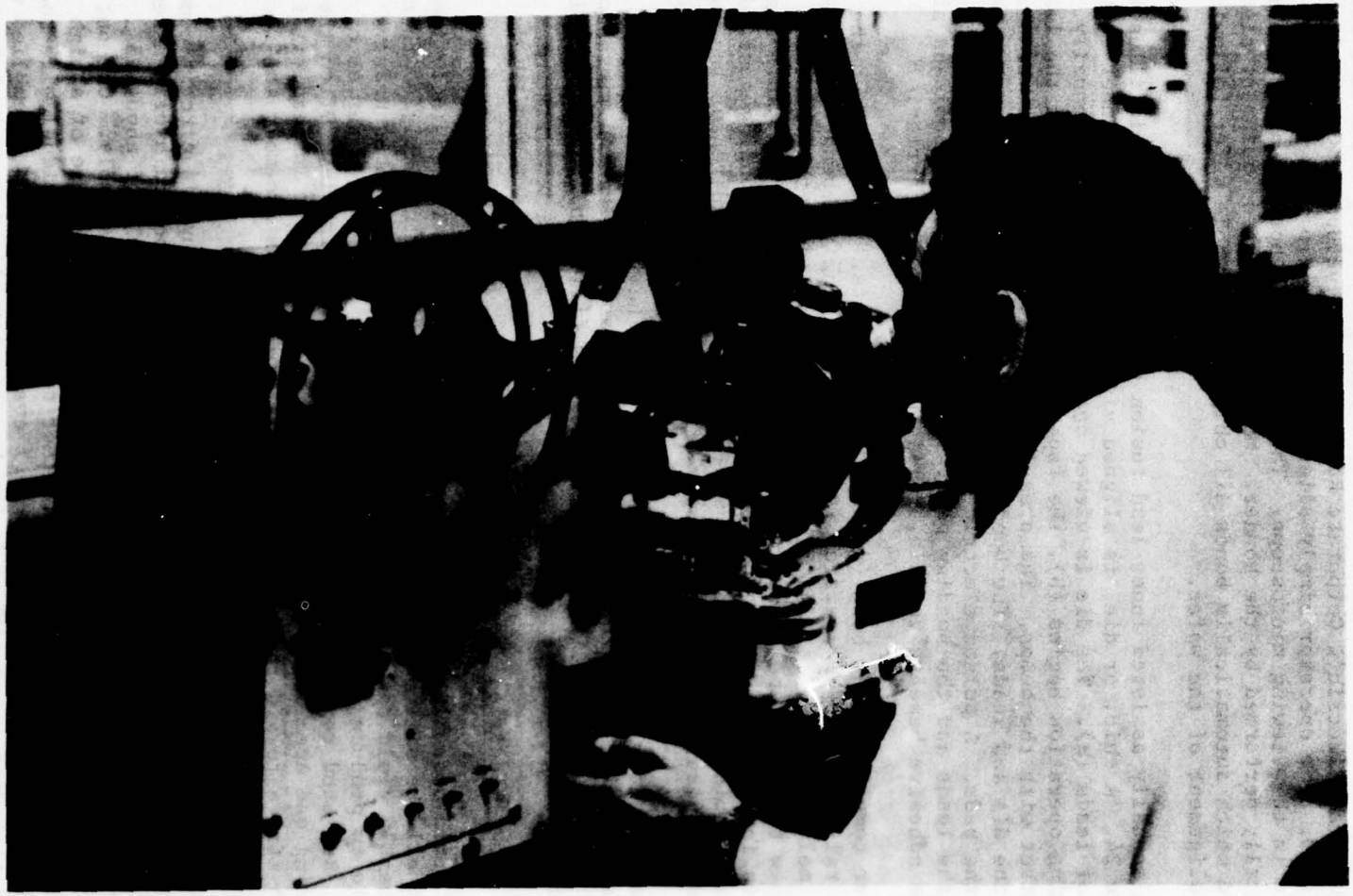
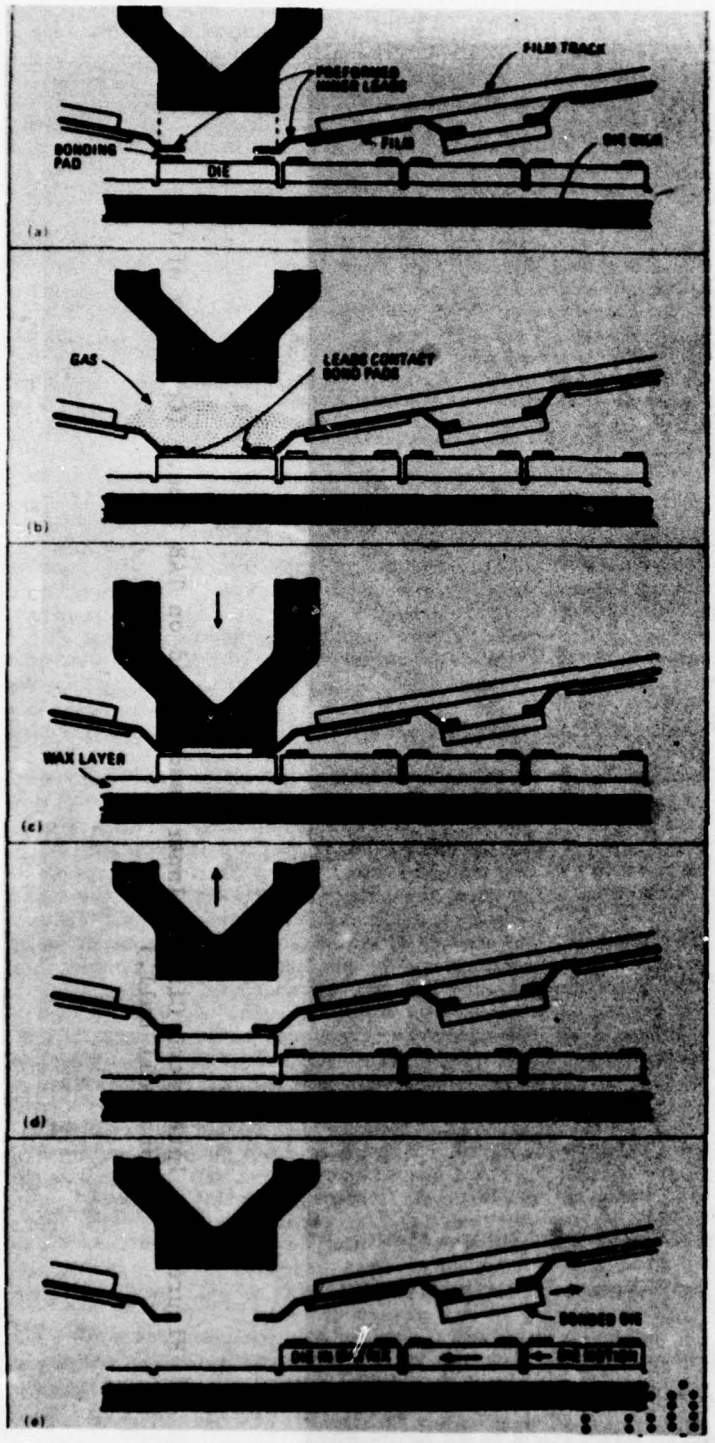


Figure 23. The Semiautomatic International Micro Industries Inner Lead Bonder Used at General Electric Corporate Research and Development.



(a)

Alignment of Chip to Leads.

(b)

Leads Positioned for Bonding.

(c)

Bonds Formed with Pulse-Heated Tool.

(d)

Chip Released with Tape.

(e)

Tape Indexed, Ready for Next Chip.

Figure 24. The Inner Lead Bonding Operation.

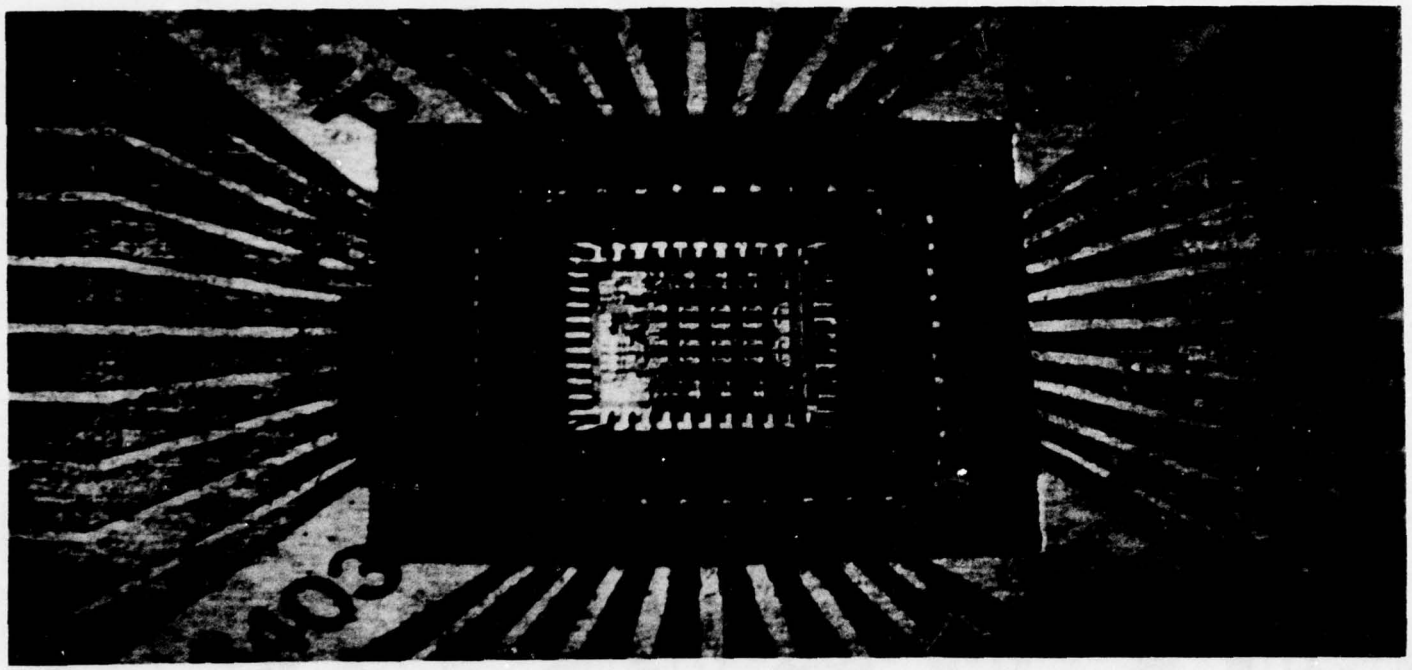


Figure 25. Integrated Circuit Inner Lead Bonded on TAB Tape. (Courtesy of CII Honeywell Bull.)

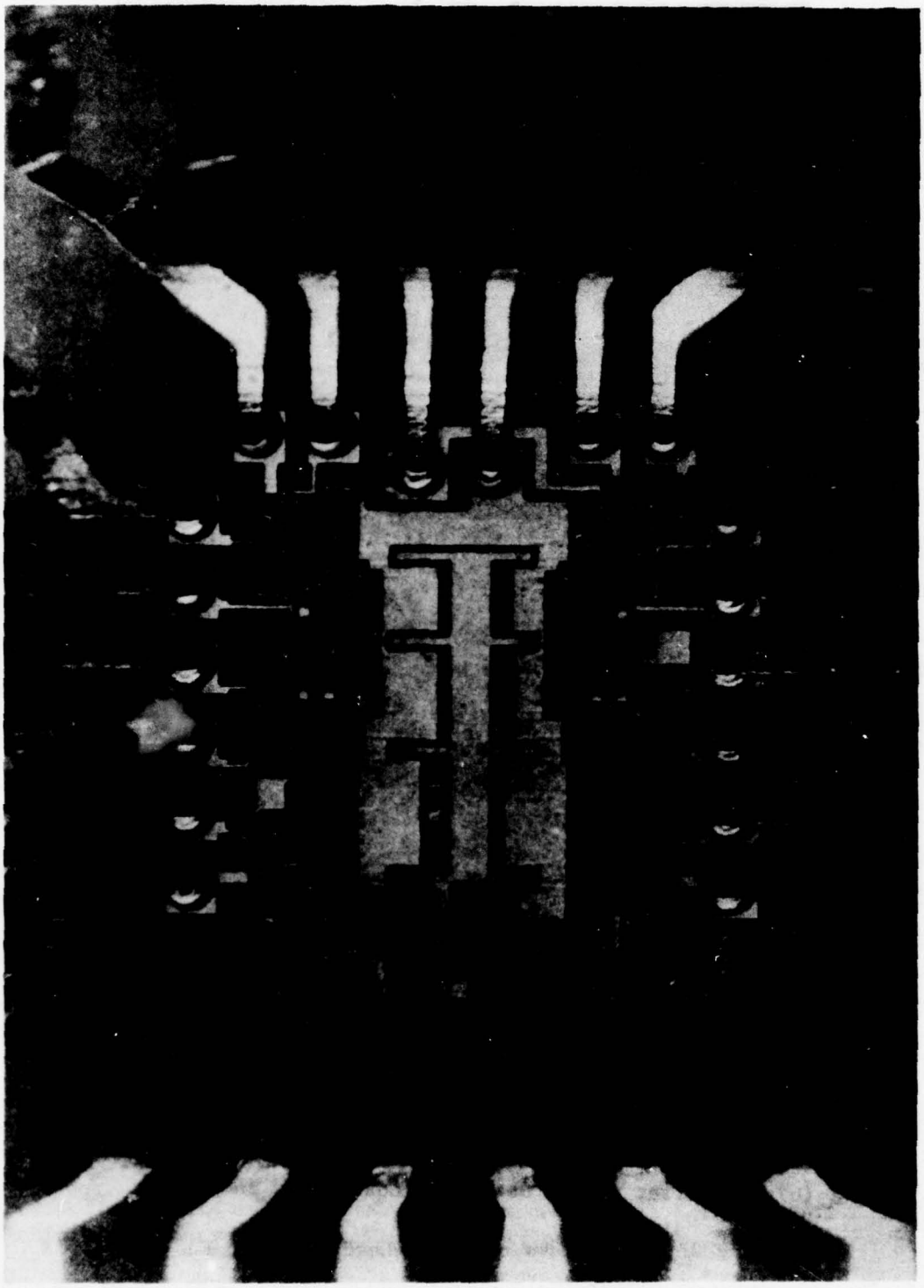
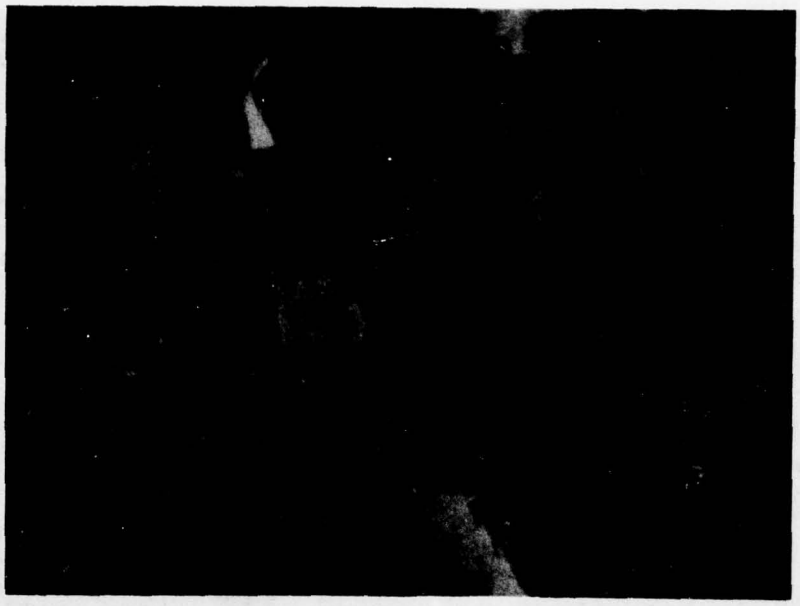
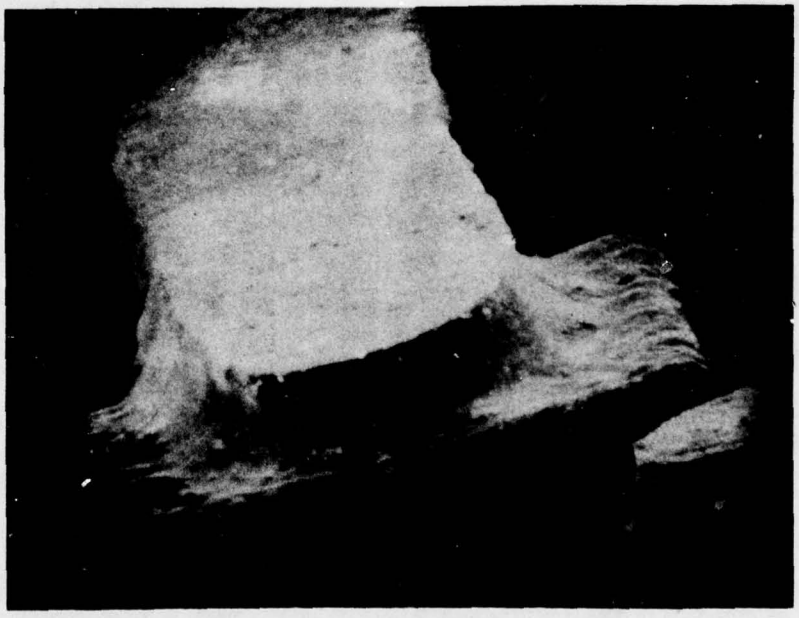


Figure 26. Inner Lead Gold-Tin Fusion Bonds. (Courtesy of CII Honeywell Bull.)



(a) Clearance Between Leads and Chip Surface.



(b) The Fillet Formed Between a Lead and a Bump.

Figure 27. SEM Views of Inner Lead Gold-Tin Fusion Bonds.

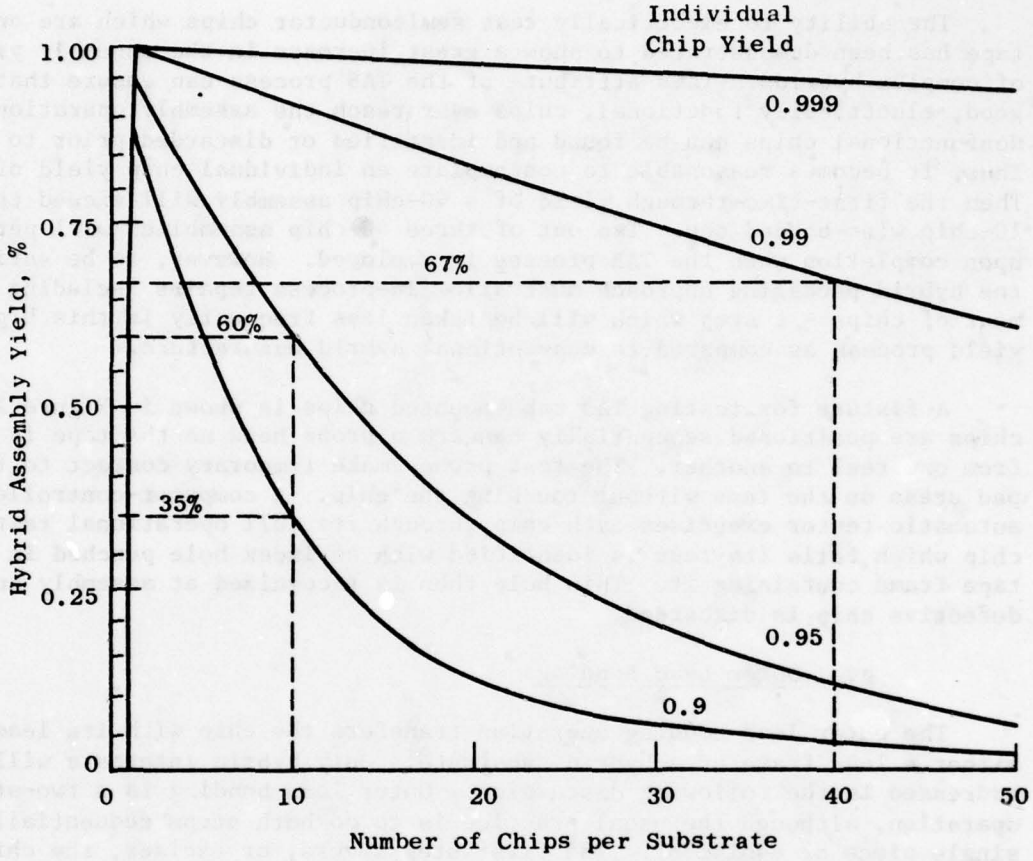


Figure 28 The Effect of Chip Density on the Yield of Complex Hybrid Assemblies.

consider more complex assemblies containing, say, 40 chips because of the low yield. Clearly, then, some way must be found to improve the yield of individual chips to make the assembly of very complex hybrid assemblies practical.

The ability to electrically test semiconductor chips which are on a TAB tape has been demonstrated to show a great increase in the assembly yield of complex hybrids. This attribute of the TAB process can ensure that only good, electrically functional, chips ever reach the assembly operation. Nonfunctional chips can be found and identified or discarded prior to assembly. Thus, it becomes reasonable to contemplate an individual chip yield of 99%. Then the first-time-through yield of a 40-chip assembly will exceed that of a 10-chip wire-bonded one. Two out of three 40-chip assemblies will perform upon completion when the TAB process is employed. However, to be satisfactory, the hybrid packaging approach must allow in-process repairs including replacement of chips - a step which will be taken less frequently in this high yield process as compared to conventional hybrid manufacture.

A fixture for testing TAB tape-mounted chips is shown in Figure 29. The chips are positioned sequentially beneath a probe head as the tape is conveyed from one reel to another. The test probes make temporary contact to the test pad areas on the tape without touching the chip. A computer-controlled automatic tester exercises each chip through its full operational test. A chip which fails its test is identified with an index hole punched in the tape frame containing it. This hole then is recognized at assembly and the defective chip is discarded.

g. Outer Lead Bonding

The outer lead bonding operation transfers the chip with its leads to either a lead frame or a hybrid substrate. Only hybrid interests will be addressed in the following discussion. Outer lead bonding is a two-step operation, although the usual practice is to do both steps sequentially in a single piece of equipment. The first step severs, or excises, the chip and its leads from the tape shown schematically in Figure 30. Then, the leaded chip is transferred to the substrate in a way that precisely maintains the original positional relationship of the chip to its tape sprocket holes. Thus, the chip will be placed on the substrate at a posiion that is known accurately. This feature makes it feasible to preposition the substrate bonding site at the exact place where the chip will arrive. Hence, the excising and placement of the chip can be fully mechanized.

A secondary lead-shaping function may be included as part of the chip excision. In hybrid applications, the TAB leads must connect from the chip surface downward to the substrate surface. Figure 31 shows a TAB-mounted chip on a hybrid substrate. The active surface of the chip is 0.008 to 0.012 inch above the substrate. The TAB leads must be shaped to sweep down to substrate level without shorting to the electrically active edge of the chip. This is accomplished by shaping the leads carefully as shown in Figure 32. The clearance between the lead underside and chip surface is visible.

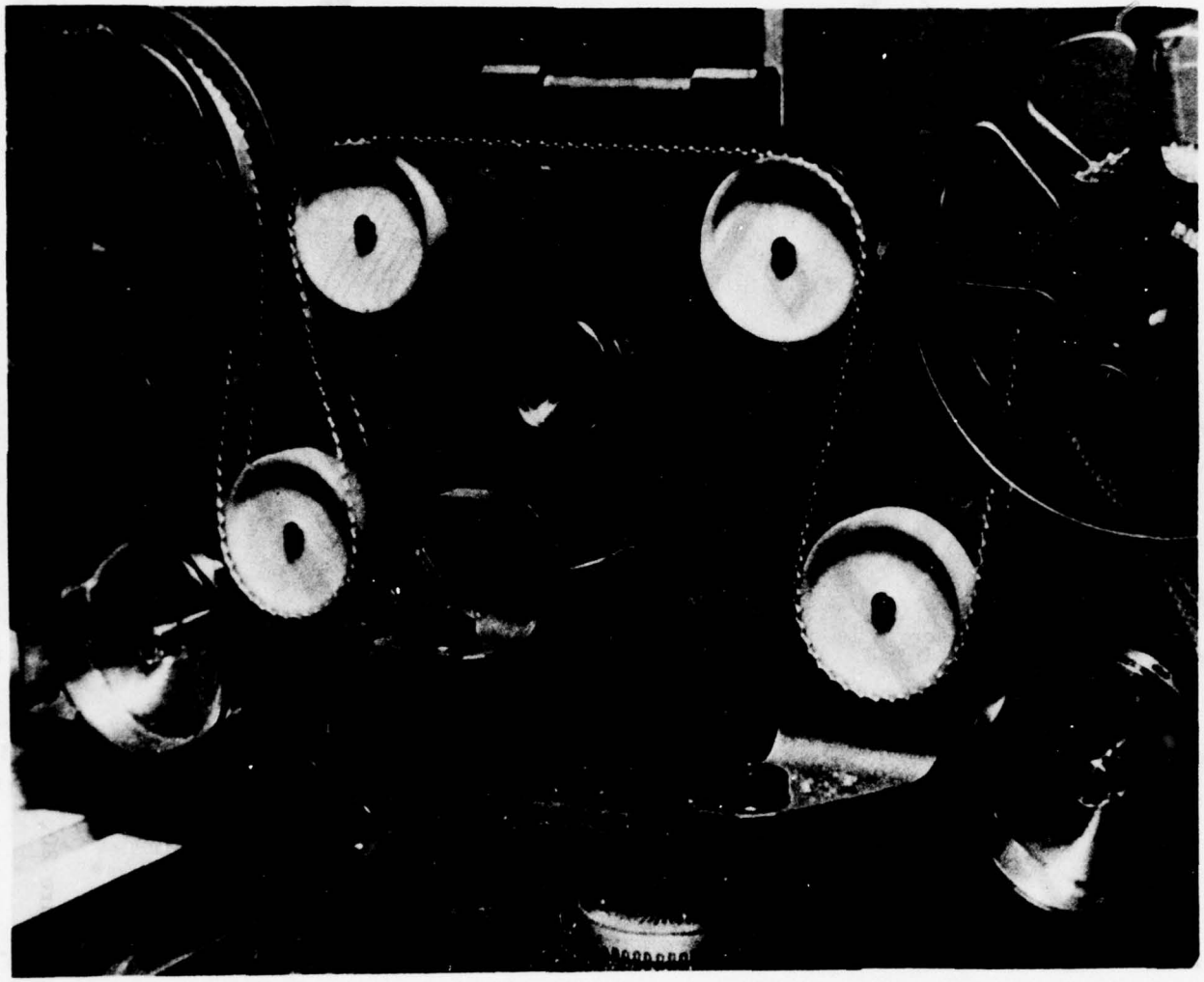


Figure 29. The TAB Tape Handler for the Automatic Electrical Testing of Tape-Mounted Integrated Circuits. (Courtesy of CII Honeywell Bull)

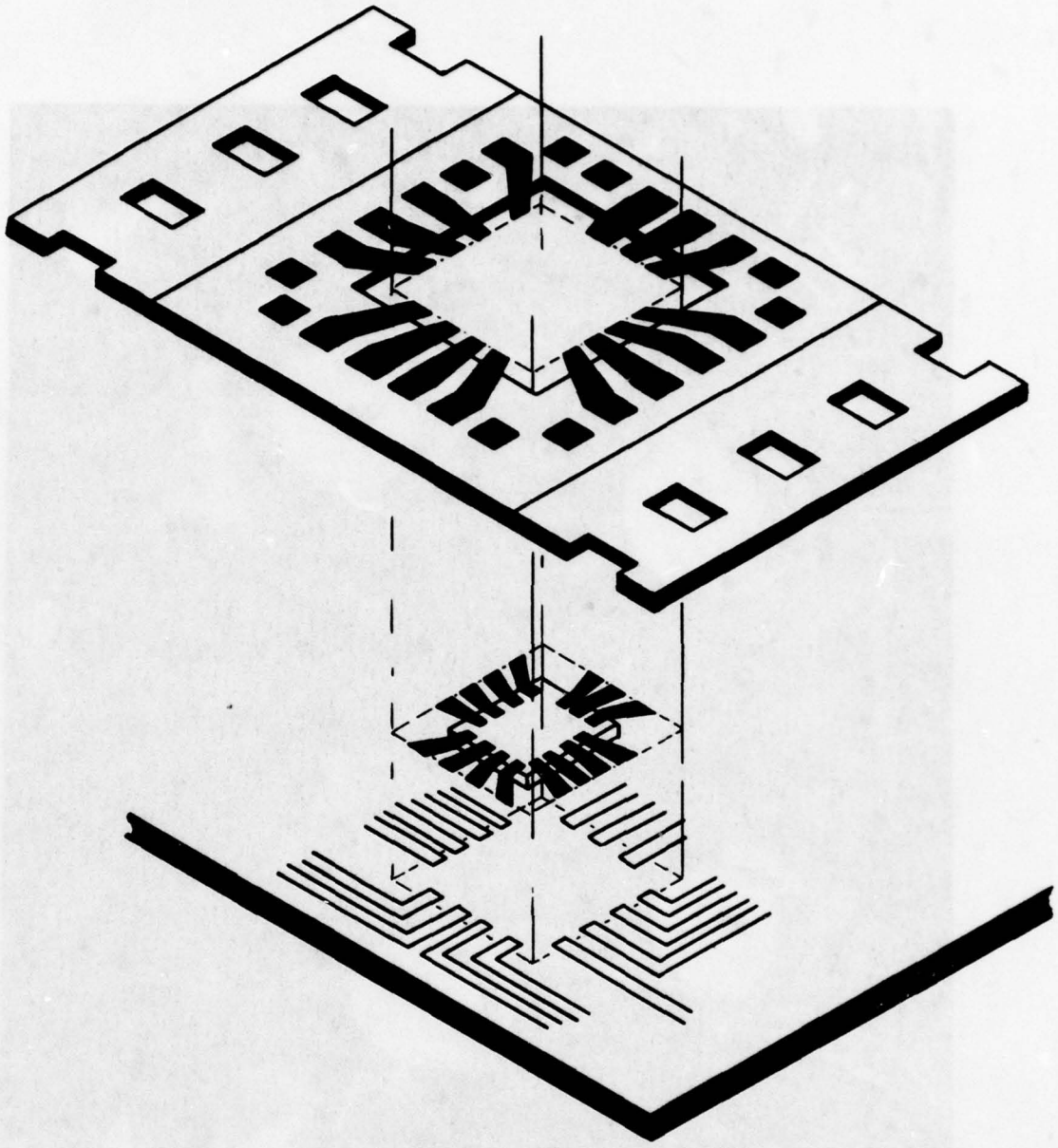


Figure 30. Schematic Representation of the Excise and Place Function of Outer Lead Bonding. The Chip with its Leads is Transferred from the Tape to the Substrate.

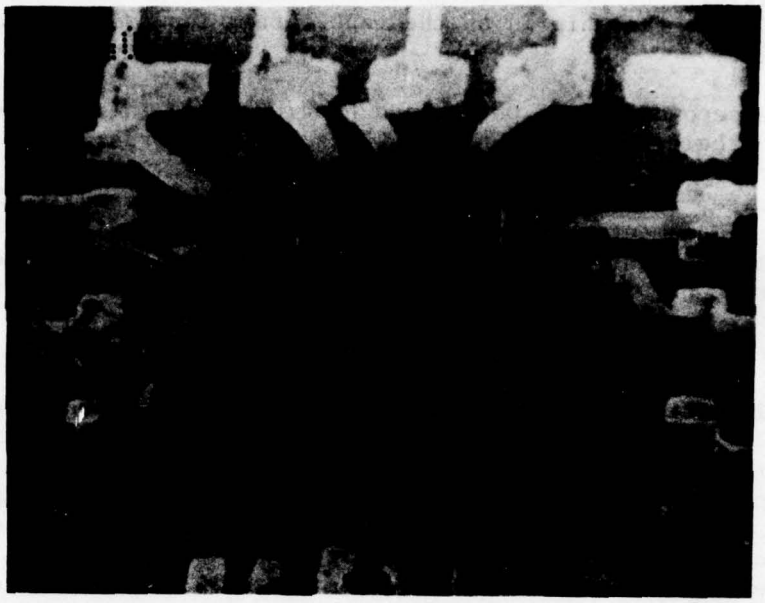


Figure 31. SEM View of a TAB-Bonded Chip on a Hybrid Substrate.

Figure 32. SEM View of TAB Leads Shaped to Avoid Shorting to the Chip as They Descend to Substrate Level.

Alternatively, by proper design of the TAB lead geometries, lead shaping can be done while the chip is on the tape, after inner lead bonding as seen in Figure 25.

The second part of outer lead bonding joins the outer ends of the TAB leads to their respective bonding pads. These bonds can be made by either thermocompression or fusion methods as described in Section II.6.d. In either case, a second tooling setup is required. Usually this is provided in the same equipment which excises the chip. The bonding tool is shown schematically in Figure 33. For fusion bonding, the tool is electrically pulse-heated to cause the reflow of a solder alloy. Frequently, this solder is applied by screen printing a pattern of paste solder on the die bond and the outer lead bonding pads.

A laboratory or pilot production scale outer lead bonder is shown in Figure 34. A substrate is placed on the holder, and a bonding site is aligned to a reference graticule in the optical viewer. The stage is moved beneath the placement tool head and detented. A single frame of tape containing the chip is inserted into the placement head. Then the bonder excises this leaded chip and lowers it into the preplaced paste solder. The stage is moved beneath the bonding head and detented. The bonding tool descends to make the bond, after which the stage is returned to the viewing position to select the next bonding site. This sequence is repeated to fully populate the substrate.

A given pair of placement and bonding tools can accommodate a reasonable range of chip sizes or different numbers of connecting leads. Only a variation in design of the TAB tape lead configuration is required for the range of different chips used with a particular pair of tools. Thus, only a few tool pairs are required even for a complex hybrid assembly. Placement and bonding tool heads are easily interchangeable on the bonder and require no alignment when exchanged.

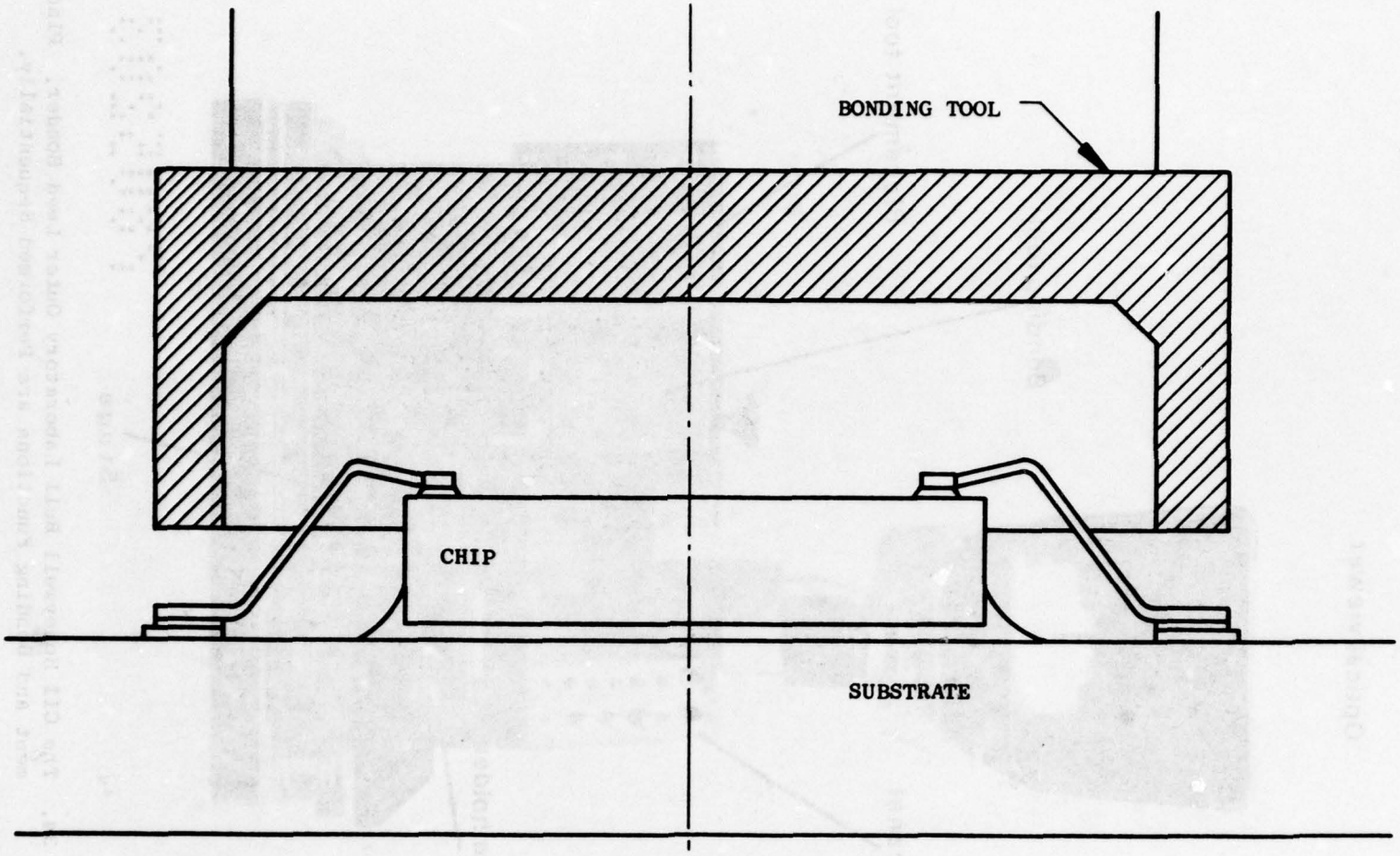


Figure 33. Schematic Representation of the Outer Lead Bond. A Hollow Tool Bonds All Leads Simultaneously.

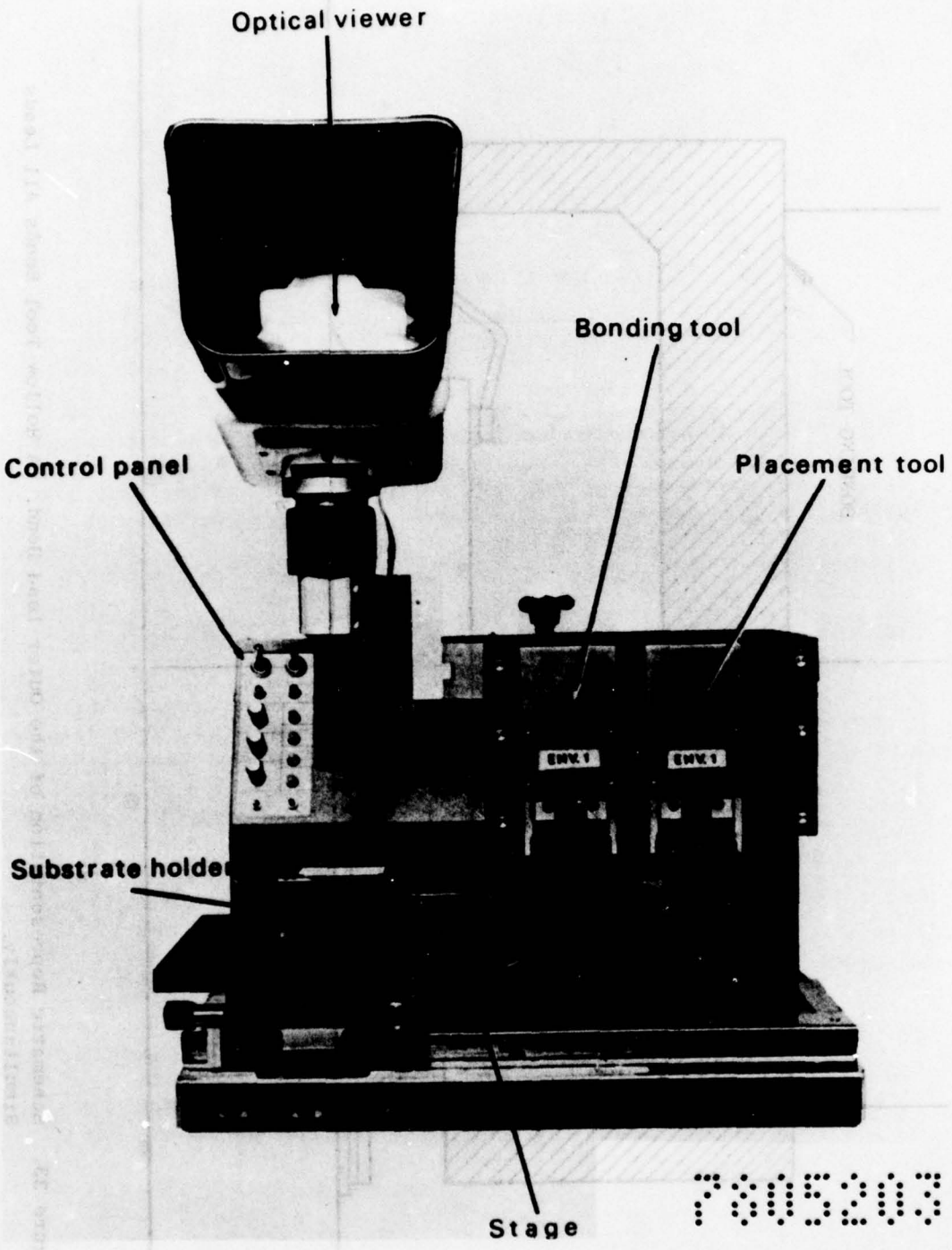


Figure 34. The CII Honeywell Bull Laboratory Outer Lead Bonder. Placement and Bonding Functions are Performed Sequentially.

SECTION III

FABRICATION AND PROCESSING

1. Memory Module Substrate

A multilayer ceramic substrate, Figure 35, was designed for the memory module circuit of Figure 4. It was fabricated by Ceramic Systems, San Diego, California, as described in Section II.4.a.3. The overall substrate size is 2 inches wide × 2-3/4 inches long × 0.050 inch thick. A central raised metallized ceramic sealing rim, 2 inches square × 0.10 inch wide × 0.040 inch high, is an integral part of the substrate such that the substrate becomes the package when covered. Also included in the substrate are five recesses, or wells, into which the integrated circuits were later assembled. The function of these wells is discussed later in Section III. The ceramic is 94% alumina, opaque black to avoid problems with light-sensitive silicon devices. The basic metallization is tungsten.

Along each narrow end of the substrate are 19 Kovar input/output pins. Some initial substrates were equipped with the 0.020 inch-diameter pins (as shown in Figure 35) as an expedient while awaiting availability of the final 0.045-inch-square pins for wrapped wire connections. All the exposed tungsten metallization was plated with electroless gold prior to silver brazing the nailhead pins in place. After brazing, the pins and the seal ring were first electroplated with nickel and then electroless gold for good solderability.

A schematic cross section of the substrate is shown in Figure 36. Although monolithic and inseparable after firing, the substrate can be considered to consist of four planes of ceramic. The lower one, CP3, is 0.030 inch thick, and its upper surface becomes the base of the chip well. The upper two planes, CP2 and CP3, are each 0.010 inch-thick. Their upper surface becomes the top surface of the substrate. An additional ceramic layer 0.040 inch-thick provides the raised seal rim. The chip wells and the seal ring are formed in their respective planes by simply punching appropriate holes in the initial green tapes prior to laminating them.

Within the substrate there are two planes of buried conductors. The lower buried layer, MP3, is between CP2 and CP3 and includes the die bond pads in the bottom of the chip wells. The upper buried layer, MP2, is between CP1 and CP2, but it is not visible. The top surface conductor layer, MP1, provides the input/output (I/O) pin attachment and integrated circuit connecting lead attachment pads. Connections among the three planes of metallization are made through vias provided in the ceramic planes CP1 and CP2. The metallized area of the seal rim is connected to one of the I/O pins by a narrow conductor band, visible in Figure 35, to electrically ground the cover. The individual conductor plane patterns are shown in Figure 37.

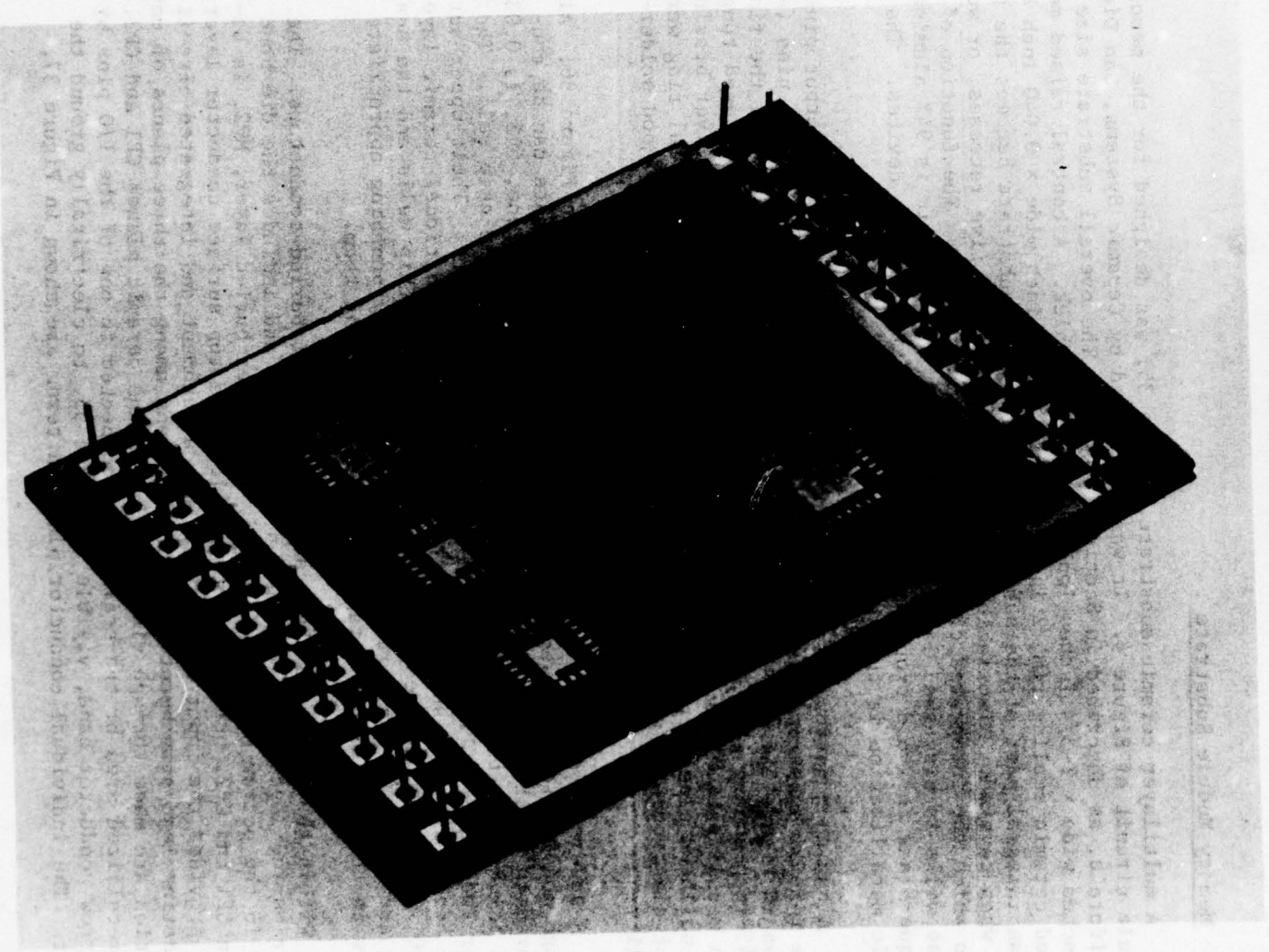


Figure 35. Early Multilayer Ceramic Memory Module Substrate Fitted with Round Connection Pins.

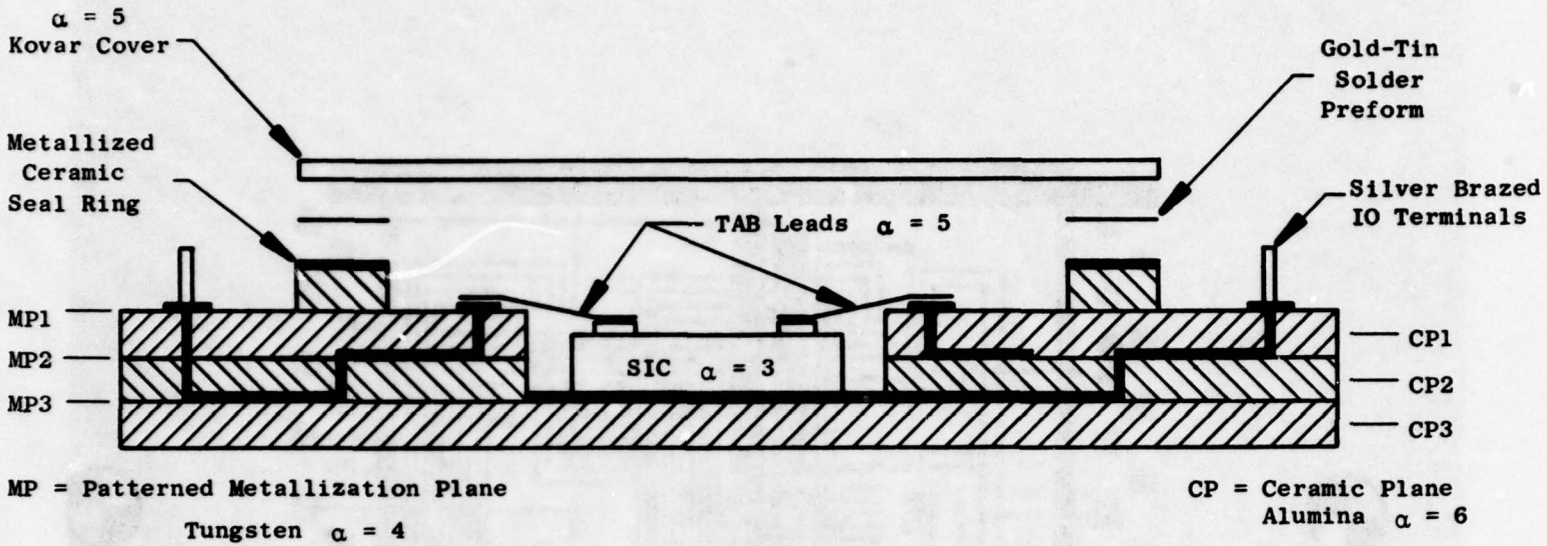


Figure 36. Schematic Cross Section of Memory Module Substrate. The Symbol α Indicates the Thermal Expansion in cm/cm/° C x 10^{-6}.

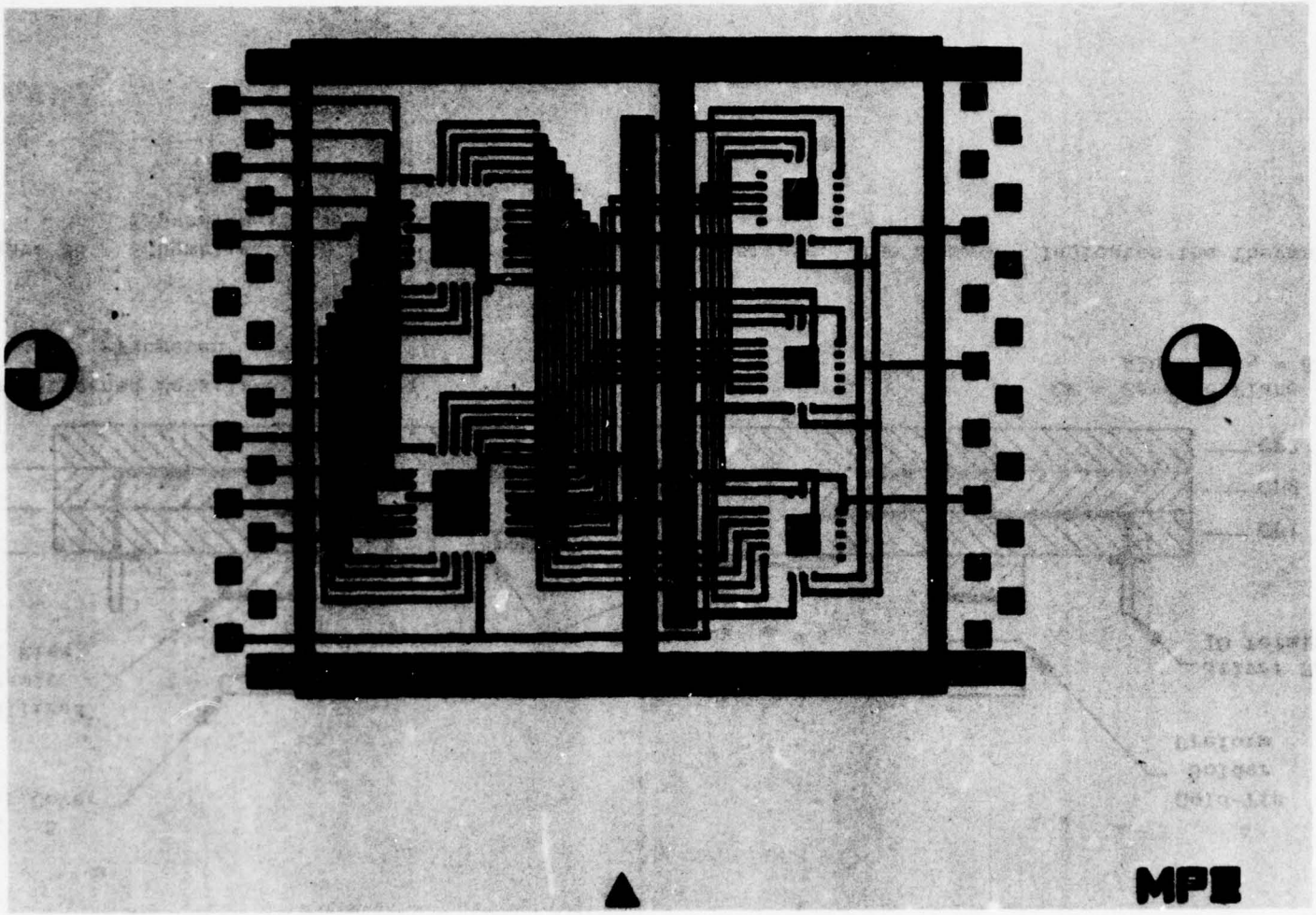


Figure 37. The Individual Metallization Layers of the Memory Module Substrate.

Although the memory module is populated sparsely, the substrate design does demonstrate the feasibility of accommodating many more integrated circuits. Nearly four square inches of available substrate area are contained within the seal ring. It is expected that as many as 25 or more integrated circuits could be contained within this package. Additional layers of buried conductors could be included easily with minimum increase in the substrate thickness. Good heat transfer from the integrated circuits is afforded by the relatively high thermal conductivity of the alumina, 2.85 kW/m^2 - ° C.

A final substrate assembly is shown in Figure 38 along with the TAB tape for the Fairchild binary counter chip used in the assembly. These substrates were fitted with Kovar connection pins 0.045 inch square and 0.400 inch long, which indirectly created two problems - one related to cover sealing and the other to pin adhesion.

It was discovered later, during assembly and test, that some pins broke off some of these substrates with distressing ease. Discussions with the vendor disclosed a brazing problem as the cause of the frequently poor pin attachment strength. The vendor explained that these pins represented a step forward in size (0.045 inch) and geometry. Some experimenting and developmental work had to be done, resulting in process improvements as the substrates were being fabricated. The final solution involved increasing the thickness of the tungsten metallization for the pin pads, over which was applied a gold strike annealed into the tungsten, followed by a thicker gold plate which also was annealed. Only the last 10 substrates were made with a process having all of these features.

Prior to using this advanced process, the pins of substrates suffering from poor adhesion were unable to survive any appreciable bending moment. Gentle handling of the substrate could result in pin failure. By contrast, substrates using the newly developed process had remarkably good pin adhesion. Destructive tests were performed on two of these substrates by noting the number of 90° reverse bends that the pins could withstand. The weakest one of the 76 pins tested survived 2 reverse bends before cohesive failure took place within the tungsten pad metallization. Three similar pad failures occurred after a minimum of 6 reverse bends. All remaining failures were breakage of the pins themselves after from 12 to 30 reverse bends.

2. TAB Tapes

All known TAB applications to date have employed copper as the lead metal. Copper has many advantages for the purpose: it offers high electrical and thermal conductivity, it adhesively bonds easily, it etches well with a good definition and etch factor, and it readily accepts electroless plating of some other metals. But, like most other metals, it has a high thermal expansion, 18×10^{-6} cm/cm/° C. This expansion is much higher than those of the other materials of construction for the hybrid package. Therefore, some other equally useful but low expansion metal had to be found for the TAB leads.

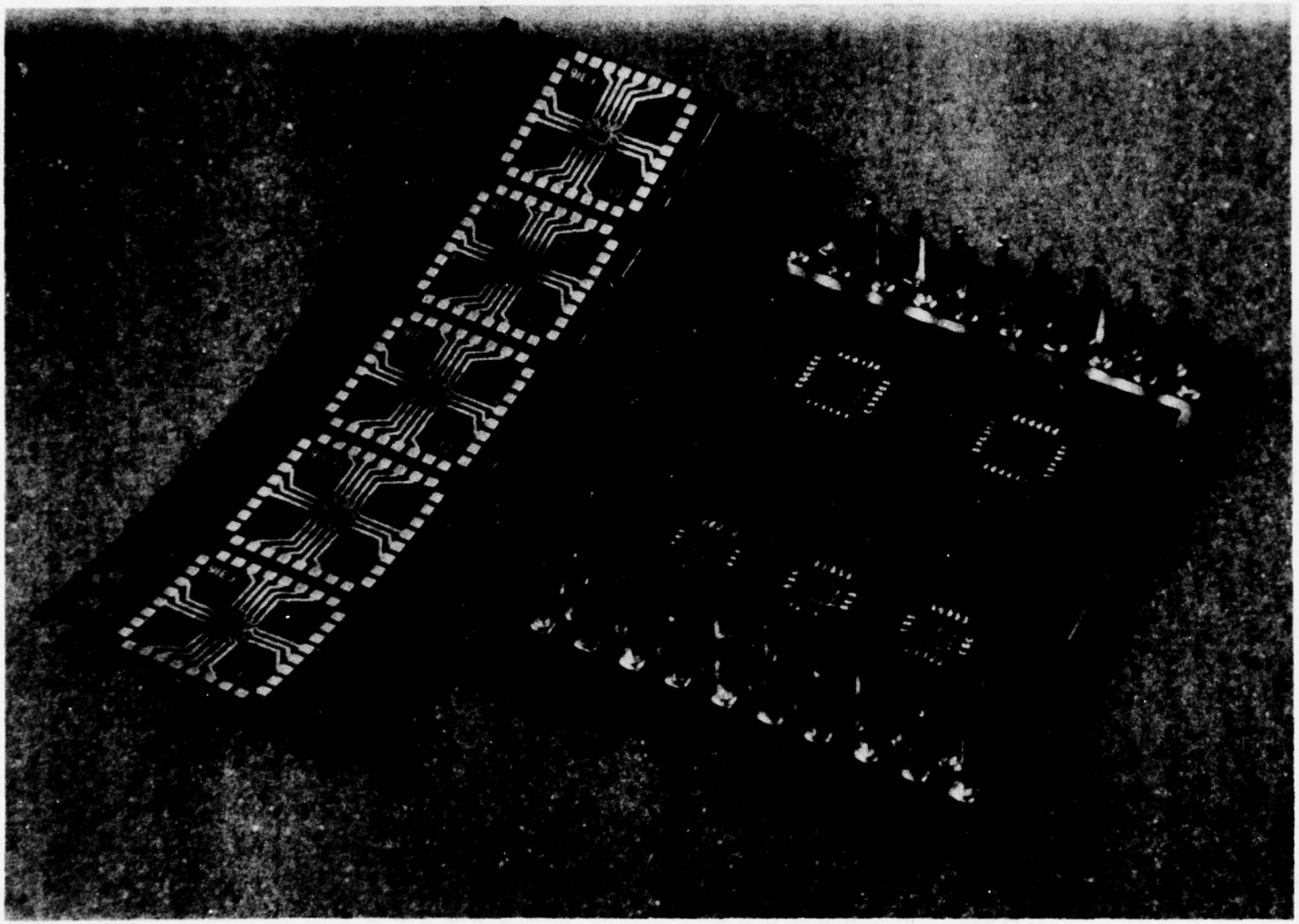


Figure 38. The Memory Module Hybrid Assembly with 0.045-inch-square Connecting Pins. Also Shown is a Length of Tape Containing the Fairchild 93S16 Integrated Circuits.

A study was made of a wide range of candidate metals alloys. Five different properties of importance were considered:

1. Melting temperature
2. Thermal expansion
3. Elastic modulus
4. Stability of the oxide
5. Etchability

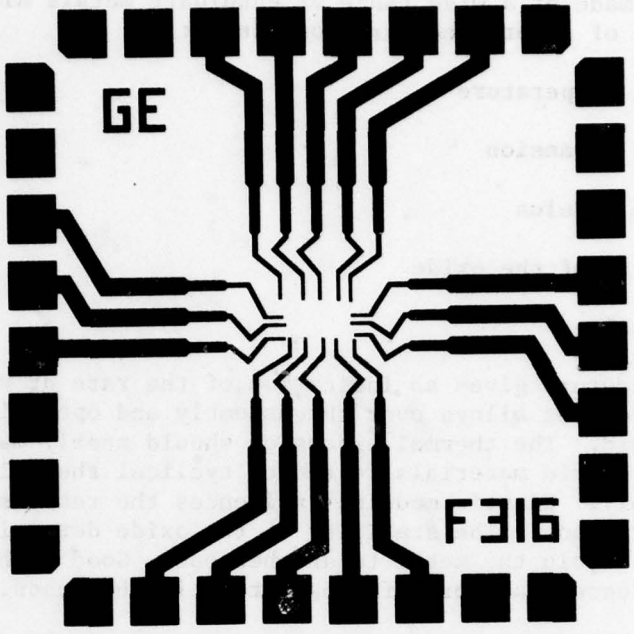
The melting temperature gives an indication of the rate at which the metal will react with joining alloys over the assembly and operating temperature range of the hybrid. The thermal expansion should nearly match the substrate and other hybrid materials to reduce cyclical thermally induced stress within the assembly. Elastic modulus influences the response of the metal to lead shaping operations. The stability of the oxide determines how easy or difficult it is to join the metal to another one. Good etchability in manageable etchants is essential for defining detail in the leads.

An iron-nickel-cobalt alloy popularly known by its Westinghouse name of Kovar® was selected as having the best overall properties for this application. The same alloy is widely available from other suppliers under various names. Its property most important to the application is a thermal expansion of 4.6 to 5.2 cm/cm/° C $\times 10^{-6}$, closely matching alumina at 6 and tungsten at 4 cm/cm/° C $\times 10^{-6}$, to 400° C. It has an elastic modulus of 20×10^6 psi, a yield strength of 50×10^4 psi, and an ultimate strength of 75×10^4 psi. It has moderately good electrical and thermal conductivity and etches reasonably well.

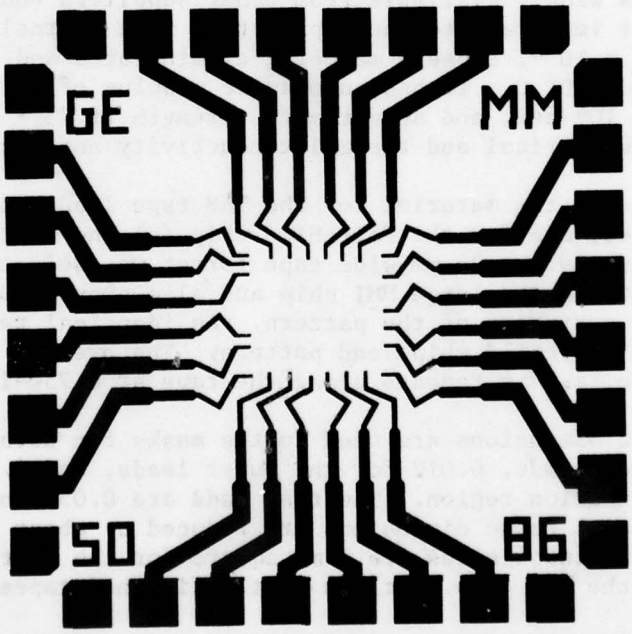
Having selected the material for the TAB tape leads, two lead patterns then were designed, one for the Fairchild chip (a) and another for the MMI chip (b) of Figure 39. A 35-mm-wide tape format was selected as being wide enough to accommodate the large MMI chip and also provide uncrowded probe test pads at the periphery of the pattern. An identical test pad pattern was included for the Fairchild chip lead pattern. The overall pattern size is 0.700 inch square, and it repeats along the tape at 0.750-inch intervals.

Similar lead dimensions are used in the masks for both patterns: 0.004 inch for the inner leads, 0.012 for the outer leads, and 0.006 inch for the intermediate transition region. The test pads are 0.055-inch square. In etching the pattern, these dimensions are reduced by about 0.001 inch by the etch factor. The window sizes are 7 mm square for the Fairchild chip and 9 mm square for the MMI chip. Frames of the finished tapes are shown in Figure 40.

One of the more critical operations in the TAB process is properly shaping the leads as they span between the inner and outer bond regions. This can be done quite successfully either while the chips are on the tape, as part of the excising operation, or in a separate operation after excising. All of

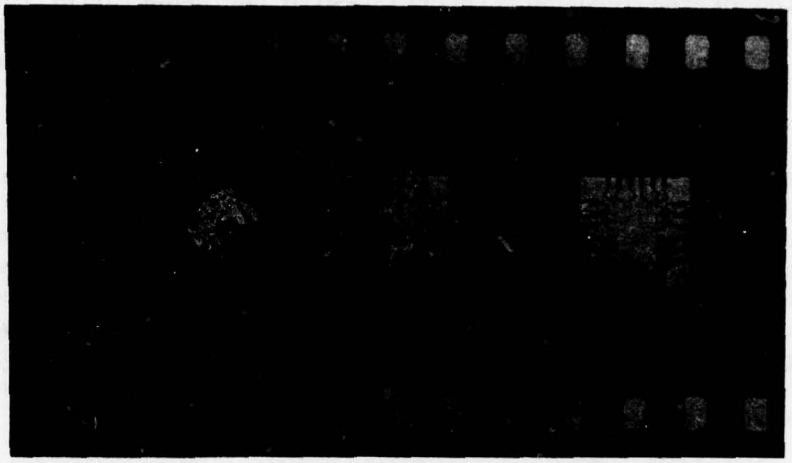


(a) Fairchild 93S16

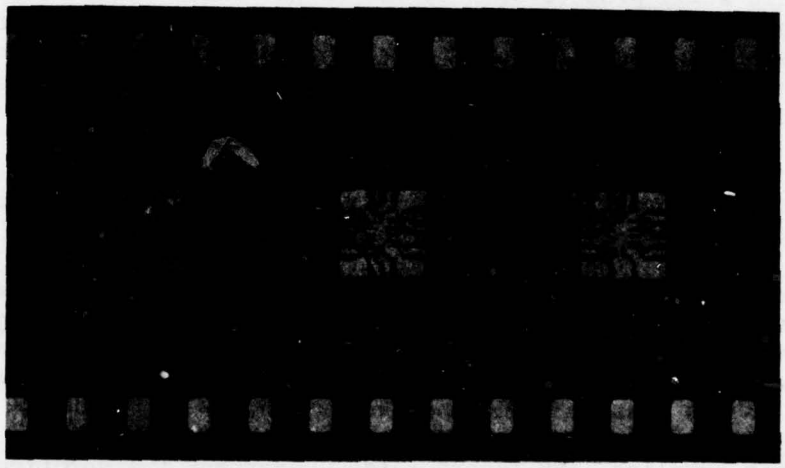


(b) MMI 5086

Figure 39. TAB Tape Lead Patterns Used in the Memory Module Hybrid Assembly.



(a) MMI 5086



(b) Fairchild 93S16

Figure 40. Lengths of Kovar TAB Tapes for the Memory Module Hybrid Assembly.

these methods require the development of precision lead shaping dies and the coordination of the lead pattern design with the behavior of the leads in the dies during their forming. The development of such dies was beyond the resources available to the hybrid packaging program and would not be cost effective for the construction of only a few test specimens.

Instead, another approach was selected, namely, the use of chip wells in the ceramic substrate. These are shown in Figure 36, the schematic cross section of the package. By placing the outer lead bonds on the ceramic surface, about 0.005 inch above the inner lead bonds, the leads sweep upward slightly as they leave the chips. This feature prevents the leads from shorting to the edge of the silicon chip and also eliminates the need for lead shaping. The use of the chip wells does add to the cost of fabricating the substrate but was the most economical approach for this program. Other applications would have to weigh carefully the merits of chip wells versus lead forming.

Although the use of Kovar for the leads more closely matches the thermal expansions among the materials of construction in the hybrid assembly, a slight mismatch still remains. Referring to the package cross section, Figure 36, it will be noted that the TAB lead bridges some distance across the alumina substrate between the inner and outer bonds. The alumina expansion is 6 and the Kovar expansion is 5×10^{-6} cm/cm/° C. This mismatch, however small, could still produce some stress in the leads and in the silicon chip if the leads ran in a straight line between their points of attachment. Both lead patterns include a feature to prevent such stress formation. Each lead includes a double angular offset in the plane of the leads, thus providing sufficient compliance to prevent significant stress generation within the leads.

The use of Kovar for the TAB leads created a number of problems which eventually were resolved with reasonable satisfaction. First, among the suppliers of normal copper TAB tapes, it was difficult to find one who would attempt to work with Kovar. Therefore, a parallel backup procurement was quickly started in copper tapes so that the assembly development phase could begin promptly. Initial copper tapes were obtained from International Micro Industries, but they were unsuccessful with Kovar. They were unable to bond the Kovar to the plastic film adhesively.

Another supplier, AMP Incorporated, undertook the solution of several difficult problems and eventually succeeded in supplying Kovar TAB tapes. The first problem, again, was bonding the Kovar to the plastic film. Rolled and annealed foil 0.001-inch-thick was used. This foil, which had a very smooth surface, required a light etch of one side for roughening to promote adhesion. The low thermal expansion of Kovar is substantially mismatched to that of the polyimide film, 20×10^{-6} cm/cm/° C. Therefore, severe warping and buckling were experienced after lamination with the common thermosetting adhesives. In fact, a substantial effort was required to develop a new, proprietary adhesive system which helped to reduce tape distortion by laminating at a somewhat lower temperature. Despite the new adhesive system, stress-induced distortion remained as a minor problem.

The unsupported Kovar foil over the window opening in the plastic has a natural tendency to "oil canning." This lack of flatness has an adverse effect upon the exposure of the photoresist used to define the lead pattern over the window. Lead pattern yield suffered because the photomask could not be brought into contact with the photoresist every time. Even the good frames suffer from a lack of planarity among the leads which makes inner lead bonding more difficult.

The tape lead patterns were designed to be electrolessly plated with tin, as required for the intended gold-tin fusion inner lead bonding. All the leads are electrically isolated. In fabricating the Kovar tapes, it was found that electroless tin did not plate onto Kovar. Two solutions were available to address this problem. One was to redesign the lead patterns for electroplating tin. This requires that all leads be electrically connected together and current buses be provided along the length of the tape. Recognizing the program delays associated with a pattern change, efforts were directed toward finding an alternate solution to the plating problem.

Electroless tin will plate on copper. Since electroless copper will plate on Kovar, electroless tin then can be deposited on the copper plating over the Kovar. This approach was followed, but the initial results were unsatisfactory. Using conventional electroless plating baths, the Kovar was first coated with copper and then with tin. Inner lead bonding could not be accomplished on these initial tapes by any combination of temperature and pressure.

A searching investigation by AMP Incorporated revealed that the tin plate was not good tin, but actually was an intermetallic consisting of both tin and copper. As such, it had a very high melting temperature, impractical for bonding. It was found that this plating became an intermetallic because of the manner in which electroless tin plating solutions operate. When plating on bulk copper, the surface copper is removed and exchanged for tin which deposits onto the copper. This exchange continues at a diminishing rate as the thickness of the tin increases. The intermediate region between the copper and tin is a combination of both metals, copper-rich near the bulk of the copper, tin-rich at the outer tin surface. With copper in copious supply for exchange with the tin, a thick layer of tin eventually covers the copper. It was discovered that the initial plated Kovar tapes simply lacked an adequate supply of copper to exchange for a useful thickness of tin.

Attempts to sufficiently increase the copper thickness using conventional electroless plating baths were unsuccessful. After the formation of an initial thin layer of copper, the deposition rate rapidly diminished to extinction on the Kovar. Again with substantial effort, AMP Incorporated successfully solved the problem through the development of a new, proprietary catalytic plating bath specifically formulated to deposit a thick layer of copper on Kovar.

The new copper plating made practical the application of a thick layer of electroless copper to Kovar. Part of this thick coating then could be exchanged for an adequate thickness of good tin for bonding. Figure 41(a) shows the cross sections of a copper-plated Kovar lead. The 190 microinch-thick shell of copper surrounding the Kovar is quite prominent. Figure 41(b) shows the cross section of the lead after electroless tin is plated over the electroless copper. The copper has been reduced in thickness to 68 microinches in exchange for the addition of 45 microinches of electroless tin. The exchange ratio of copper to tin is approximately 3:1.

Figure 41 also illustrates another technical challenge faced in the use of Kovar - a lower etch factor. The pronounced slope to the lead edges is undesirable because it makes it difficult to accurately control the lead dimensions. This is particularly important in the inner lead bonding regions because the dimensions there are necessarily small. The difference in slope between the two sides is a directional effect caused by using the spray etching method.

In summary, then, TAB leads made of Kovar have the advantage of a good expansion match for the hybrid package. Advances in process technology and a recognition of the manufacturing constraints are necessary to Kovar use. The laminating, plating, and etching processes developed here do require further refinement. Kovar lead forming properties should also be explored.

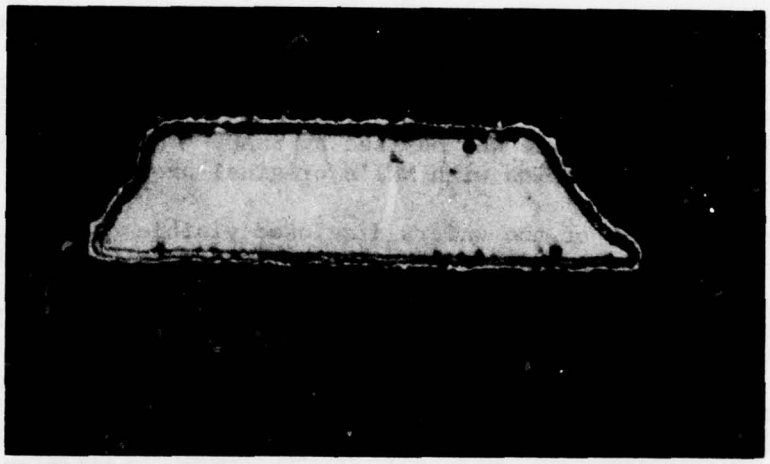
3. Wafer Processing

The hybrid module memory assembly required two different types of integrated circuits. One was an MSI 4-bit fast TTL binary counter available from Fairchild as their type 93S16. The other was an LSI bipolar read-only memory (ROM) available from Monolithic Memories, Incorporated (MMI) as their type 5086. These devices were both obtained as complete silicon wafers but each was quite different.

Fairchild is already a large-scale user of the TAB technology in manufacturing its molded plastic line of semiconductor products. The required 93S16 device was not included in that product line and, therefore, was not immediately available in TAB form. Nevertheless, Fairchild was quite willing to accept a special order from General Electric for the required 93S16 devices completely prepared and ready for inner lead bonding. In response to an order for four such wafers, Fairchild started a special wafer processing run for five wafers - the fifth being a spare. The wafers were two inches in diameter.

The five wafers were processed through Fairchild's BETA (BEam TApe) operations including gold bumping, carrier plate mounting, and diamond sawing for separation. Wafer processing defects caused rejection of three of the five wafers at Fairchild's final inspection. The two good wafers were delivered to General Electric with a yield of 47 good devices. The rejected wafers were provided free and served as a generous supply of engineering samples for bonding development.

(a) Plated with 190 microinches of Copper.



(b) Overplating with 45 microinches of Tin Reduced the Copper Thickness to 68 microinches.

Figure 41. Cross Sections of Kovar TAB Tape Leads.

The Fairchild devices required no further processing by General Electric and were ready for inner lead bonding as received. Figure 17 shows the wafer on its carrier plate as received by General Electric from Fairchild. Figure 42(a) shows a group of the devices, and Figure 42(b) shows an individual device. The chip size is 0.080 × 0.108 inch; it had 16 bumps for lead attachment.

Monolithic Memories is not active in TAB processing and, thus, could supply wafers only in the form used in their wire-bonded product line. These are conventional three-inch-diameter wafers with aluminum metallization protected by a layer of silicon dioxide. The connection pads are aluminum and designed for aluminum wire bonding. Three such wafers were ordered from MMI, to be processed for TAB bonding by General Electric.

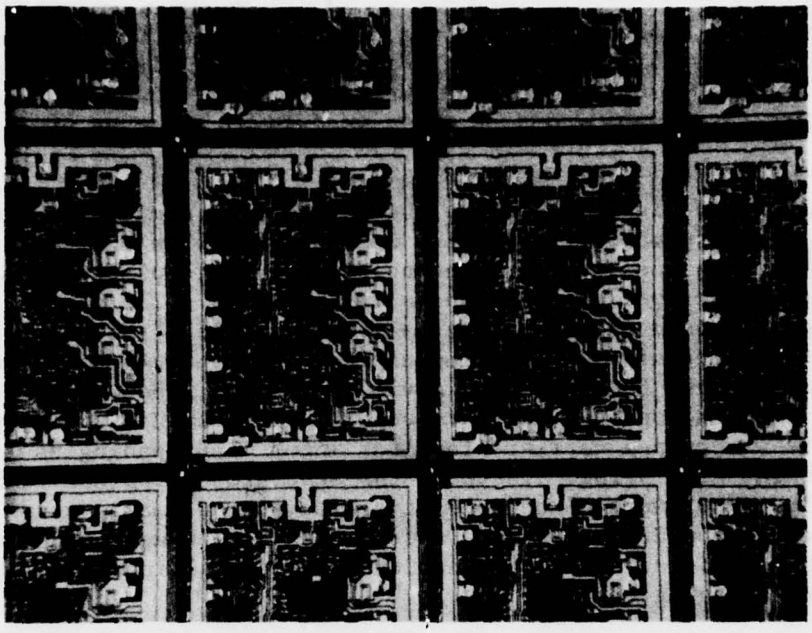
Although not an outside IC supplier, General Electric has made a Corporate commitment to maintain a custom silicon wafer processing capability with research excellence. This is the Solid State Applications Operation (SSAO) in Syracuse, New York, which has an established solder bump process for use on the custom integrated circuits it supplies to internal General Electric operations. With some modification, this process was used for providing the gold bumps on the MMI wafers.

Upon their receipt at SSAO, inspection of the wafers indicated that a total of 54 devices had passed MMI's final wafer probe test, as evidenced by inked reject devices. The wafers then were bumped and the individual devices subjected to a thorough functional test on Teradyne automatic testing equipment. The test procedure was devised by SSAO. The test results were found to bear a poor correlation with MMI's original probe test.

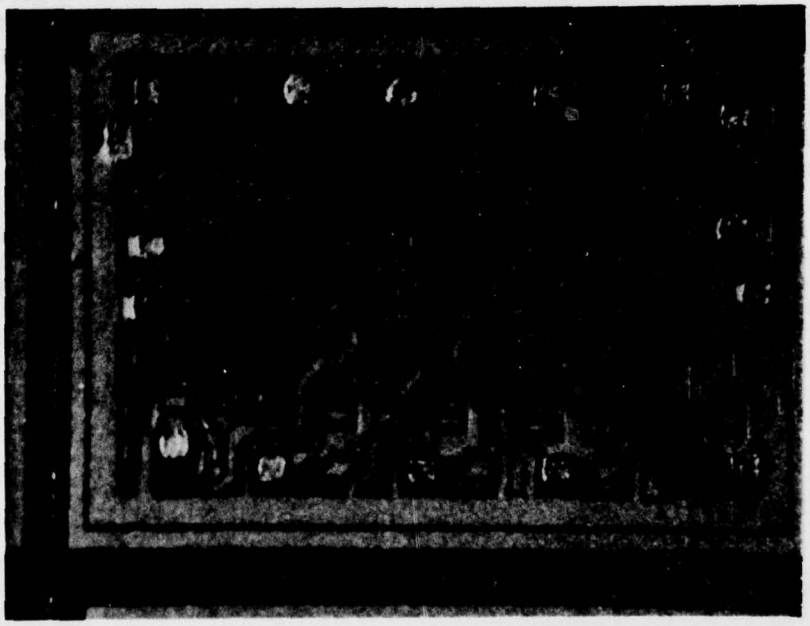
A visual study of the wafers disclosed visible defects in the original wafer processing, the results of which correlated highly with SSAO's test results. Now the potential reliability of any device taken from these three wafers was seriously questioned. In the best interests of the program, it was decided to abandon these wafers and start afresh.

Next a second lot of 6 MMI wafers was ordered on the basis of a guaranteed yield of at least 50 good devices. When received, these wafers were completely tested by SSAO, and this time there was an exact correlation with MMI's probe test yield. Three of these wafers then were gold bumped by SSAO with, surprisingly, a 100% yield. No originally good device failed after being bumped. Then, the remaining three wafers were bumped.

The SSAO gold bump process is fundamentally similar in concept to that described in Section II.6.b. A proprietary two-layer intermediate metallization is applied to the wafer to provide good adhesion and low contact resistance to the aluminum pad metallization. This intermediate metallization is photoresist coated and patterned to open windows in it over the pad areas. The bump then is built up to a 0.001-inch height with electroplated copper over which is added 0.0001 inch of electroplated gold. Then, the photoresist and the intermediate metallization are removed completing the process. No additional passivation was added to the wafers.



(a) A Portion of the Wafer Matrix.



(b) An Individual Chip in the Matrix.

Figure 42. The Fairchild 93S16 Device.

Figure 43(a) shows a portion of a MMI wafer after bumping but prior to separation. Figure 43(b) shows an individual device with its bumps. The chip size is 0.150 × 0.171 inch and the device has 24 bumps for lead attachment. Figure 44 shows a group of three individual bumps as processed by SSAO.

Two unusual design features in the MMI 5086 chip made it awkward to handle in the TAB process. The wafer was designed with unusually narrow 0.002-inch scribe lanes. Several connecting pads are placed immediately adjacent to the scribe lanes, as shown in Figure 45. The plating buildup during bumping caused one pad to actually project into the scribe lane. This made diamond sawing of the wafer impractical for separation because the saw blade could tear the bump from the device. Instead, the wafers had to be diamond scribed and snapped apart to separate the devices. This prevented mounting the wafer on a carrier plate for inner lead bonding as is the normal practice in TAB processing. Instead, the separated chips had to be handled individually. They were placed one at a time over a small vacuum holddown hole in a carrier plate for inner lead bonding. Although inconvenient, this method worked satisfactorily and permitted successful inner lead bonding for this Hybrid Packaging Program.

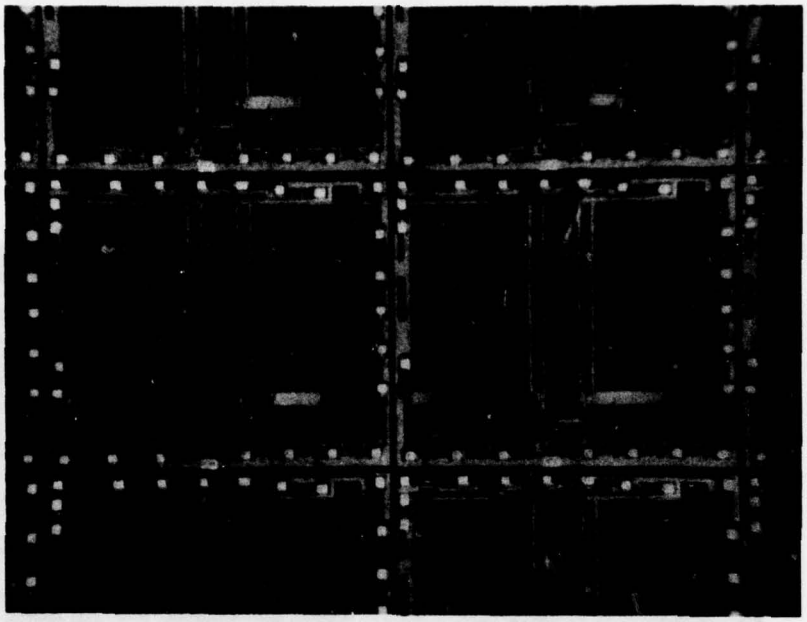
4. Inner Lead Bonding

The gold-tin fusion method was selected for inner lead bonding. A similar type of bond has been in use in General Electric's product line of plastic-encapsulated signal transistors since the product inception during the mid-1960's. Many years of product reliability data have been accumulated to verify the reliability of the gold-tin fusion bond as used in the product. For inner lead bonding, the required tin is plated onto the TAB leads and gold is present as the bump on the silicon chip.

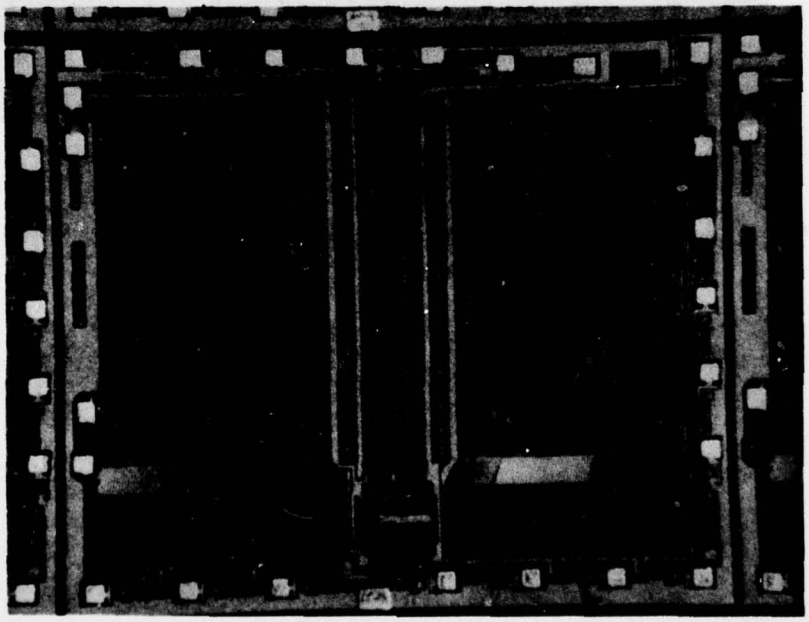
Inner lead bonding was performed with the bonder shown in Figure 23. The different dimensions of the Fairchild and the MMI chips required different pulse heating tools. Each required somewhat different operating parameters to effect good bonds as shown in Table 9.

Table 9. Inner Lead Bonding Parameters.

	Fairchild	MMI
Force, grams	250	400
Dwell Time, seconds	3	5



(a) A Portion of the Wafer Before Separation



(b) An Individual Device on the Wafer

Figure 43. The MMI 5086 Device.

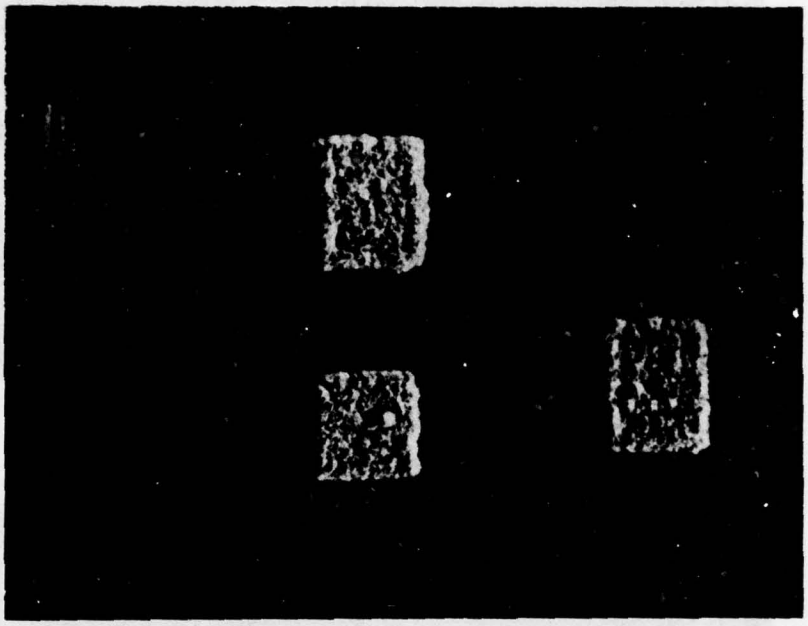


Figure 44. Part of an MMI 5086 Wafer Showing Bumps Processed by General Electric.

Figure 45. Part of an MMI 5086 Wafer Showing Close Placement of Connecting Pads to Narrow Scribe Line, Horizontal Line in Center.

The portion of the dwell time during which the tool is actually heated is only about 0.5 second. The remainder of the time allows for the tool to cool and the bond to freeze. No attempt was made to minimize the total bonding time.

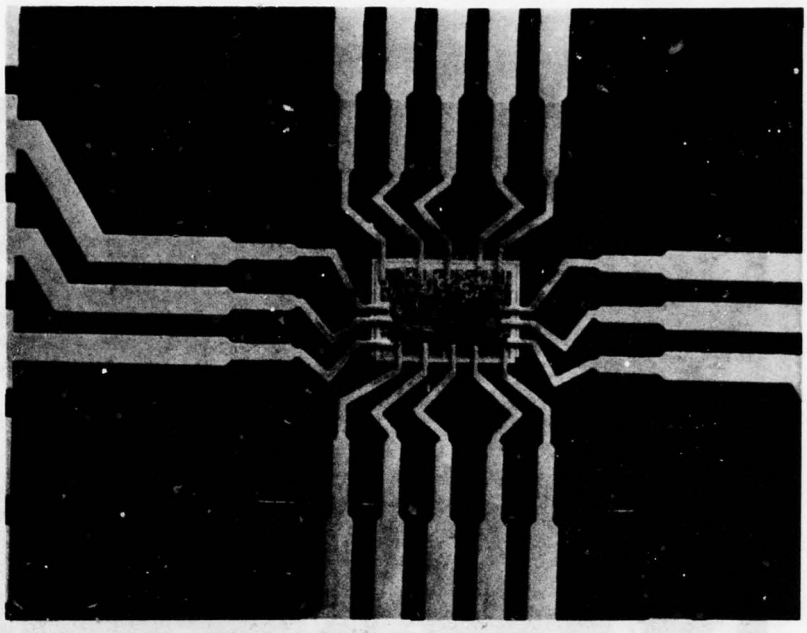
The bond quality criteria were the formation of generous, well-defined fillets of the gold-tin alloy between the edges of the leads and the gold bumps. A good correlation was found between a good fillet formation and a high bond strength. Destructive pull tests were made on many leads during the process preparation phase. Optimum bonding conditions resulted in lead breakage, requiring a minimum pull of 50 grams. Without the well-formed fillet, the lead bond to the bump would fail with little strength. In a good filleted bond made with excessive force, the failure would occur between the gold bump and the silicon of the chip itself, with visible evidence of fracture within the silicon.

One requirement for maintaining good quality inner lead bonding is the use of a clean, relatively fresh tin plating. Even in a nitrogen protective atmosphere, the maximum storage life of tin plated tapes was found to be four to six weeks. Tapes stored longer than that time failed to bond well, as evidenced by fillet formation. It finally was found best to obtain copper tapes without tin plating and to obtain the Kovar tapes plated with copper only. A laboratory tin-plating bath was established at GE to plate the tapes prior to their use for inner lead bonding. Bonding within three days of plating produced the most consistently good bonds.

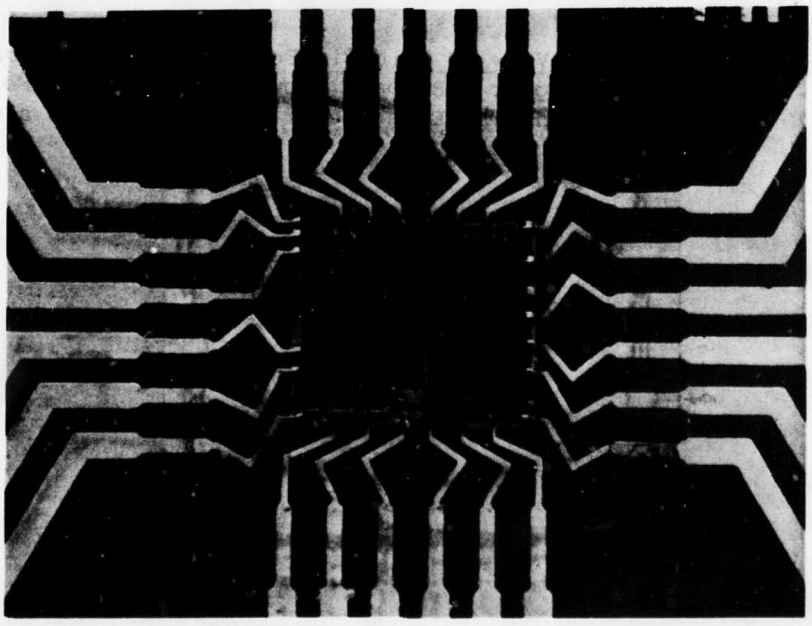
The bonded chips are seen in Figure 46; (a) is the Fairchild and (b) is the MMI. Figure 47 shows in detail two inner bonds made to Kovar leads. The good fillet formation and lead wetting is readily visible. Also, the slope of the lead edges should be noticed; this is caused by the low etch factor of Kovar.

5. Outer Lead Bonding

Simplicity and easy repairability led to the selection of solder reflow of the outer bonds. The solder alloy was selected to have a low solubility for gold, thus protecting the gold plating over the tungsten bonding pads. It should be soft and ductile, yielding during temperature cycling to minimize stress within the joint. The lead-indium family of solder alloys was considered best qualified to meet these requirements. Lead and indium form a solid solution. Thus, an alloy with a working temperature ranging from indium at 157° C to lead at 327° C can be selected, depending upon the proportions of the components. A 50% lead/50% indium alloy with a melting temperature of 215° C was chosen. This temperature is sufficiently below that used for inner lead bonds to avoid disturbing this completed bond during the subsequent outer lead bonding operation. The choice of the 50% lead/50% indium solder also was influenced by its good performance during temperature cycling of the TAB test substrates, as described in Section V.1.



(a) Fairchild 93S16.



(b) MMI 5086.

Figure 46. Chip Inner Lead Bonded to Kovar TAB Tapes.

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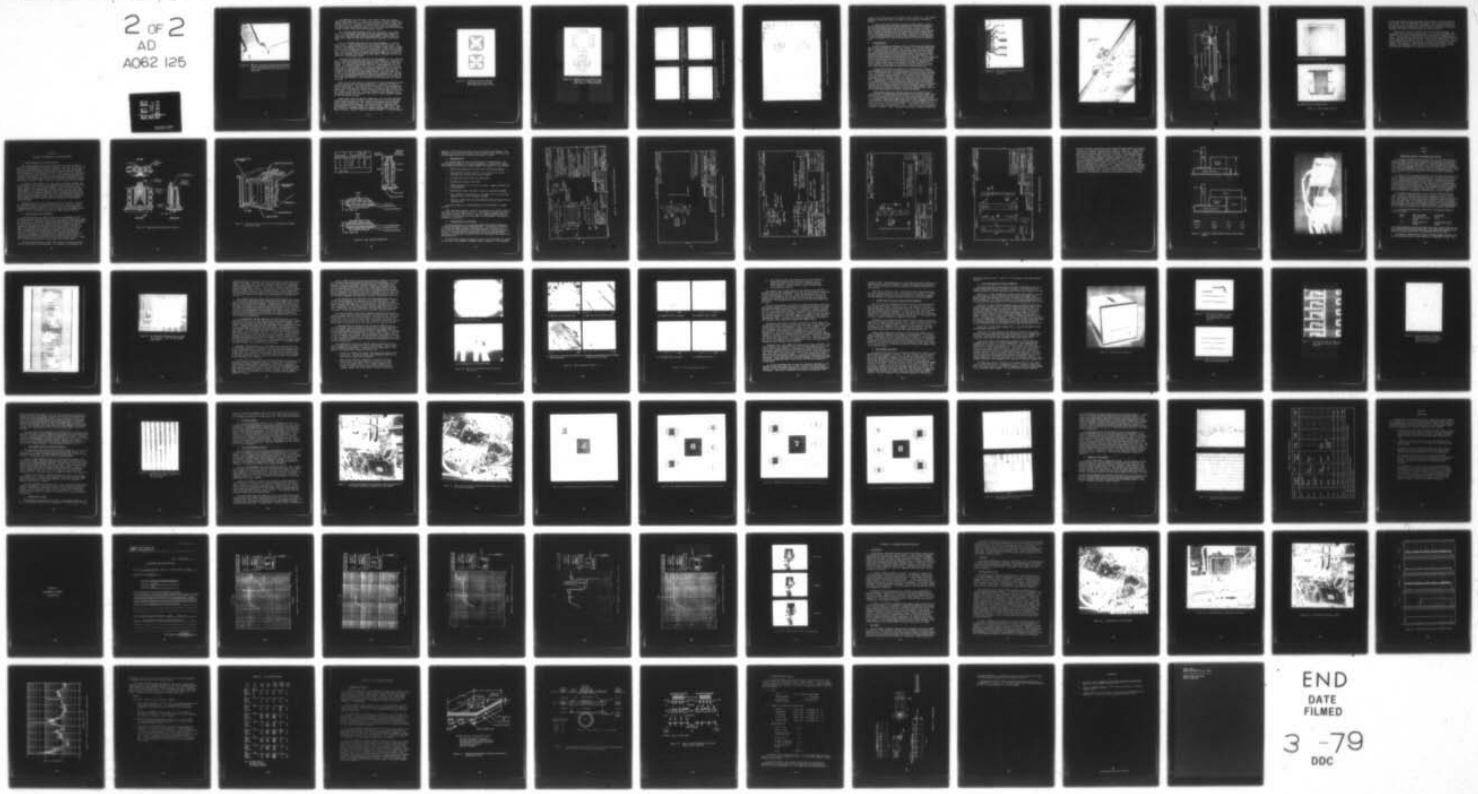

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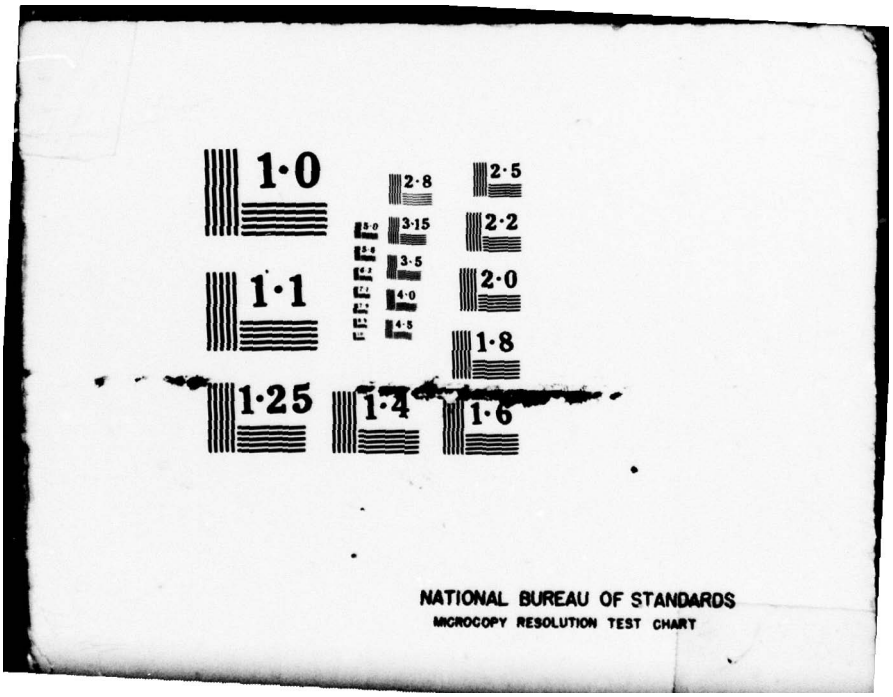
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MICROCOPY RESOLUTION TEST CHART

Figure 47. SEM View of Gold-Tin Fusion Inner Lead Bonds to Kovar TAB Leads Showing Good Fillet Formation. The Etch Factor of the Kovar is also Noticeable.

The assemblies were made using a 50% lead/50% indium paste solder, duPont Formon number 9567. A paste solder consists of finely divided alloy powders dispersed in an organic vehicle system which contains a solder flux. The mixture has the consistency of a medium paste, hence its designation. The paste solder was applied by means of an air-pressure-operated dispensing syringe through a blunt, small-bore hypodermic needle.

The subsequent hybrid assembly steps were done by hand using simple aids. The tape-mounted chips, Figure 48, were prepared for assembly by cutting the leads free just inside the window edges. Excised chips with their leads, Figure 49, then were handled with a soft-tip, vacuum-pickup pencil.

The first assembly operation was the solder attachment of the gold-backed chips to their bonding pads in the bottoms of the chip wells. The substrate was prepared for this operation by placing a small amount of paste solder on each bonding pad as shown in Figure 50(a). A chip then was placed into the solder in each well and its lead aligned to the outer lead bonding pads. Since the well depth was greater than the thickness of the chip, the chips were suspended over the wells by their leads. The chips were held in position by the wet paste solder.

To depress the chips into the wells, the arrangement of Figure 50(b) was used. A small block of Teflon was placed on top of each chip. Light coil springs then were stretched between substrate pins, in line with the Teflon blocks. By sliding the springs down the pins, a small downward force was exerted on the Teflon blocks. This force, in turn, pressed a chip onto the paste solder on its bonding pad. The substrate then was placed as shown on a temperature-controlled hot plate operating at 225° C. After about 10 seconds on the hot plate, the paste solder melted. With the solder melted, the force from the springs seated the chips on their bonding pads. The substrate then was removed from the hot plate and allowed to cool, bonding all five chips simultaneously. The springs and Teflon blocks then were removed for reuse.

Then, all the outer leads on a substrate were bonded simultaneously with a second, similar, hot-plate-heating operation. Preparation for this is shown in Figure 50(c). The paste solder was placed in a line extending over all the outer leads and their bonding pads, including the space between the bonding pads. The substrate then was returned to the hot plate to cause this paste solder to melt and flow. The chip attachment solder melted too, but its surface tension force maintained each chip in correct alignment throughout the heating and cooling.

Figure 50(d) shows the substrate immediately after the outer lead bond solder operation, before cleaning. Surplus solder can be seen on the substrate between bonding pads. This surplus is nonadherent and was removed easily during substrate cleaning. The substrates were cleaned in three successive baths of duPont Formon flux residue remover, number 8529. This was followed by a thorough washing in flowing deionized water and an oven bake for drying. Figure 51 shows the completed assembly. A close-up view of

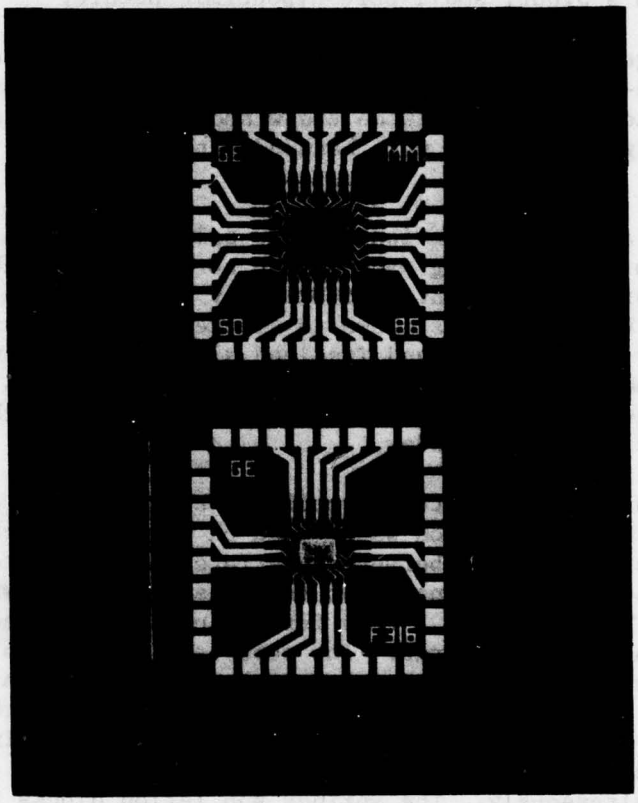


Figure 48. Individual Frames of TAB Tape Containing Chips; (Top) MMI 5086, (Bottom) Fairchild 93S16.

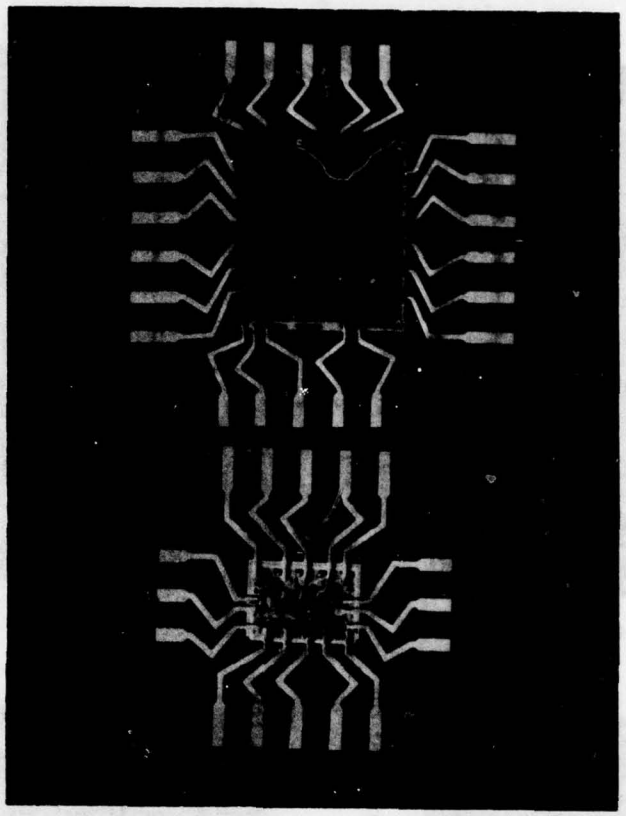
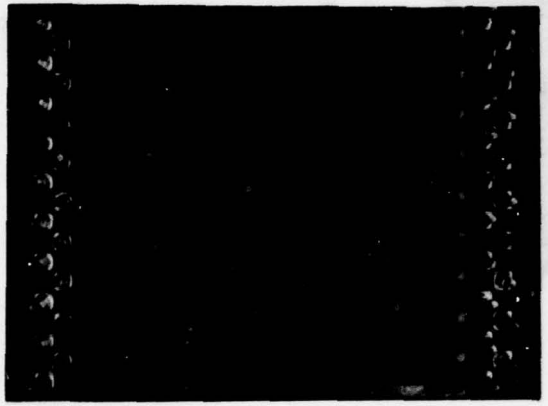


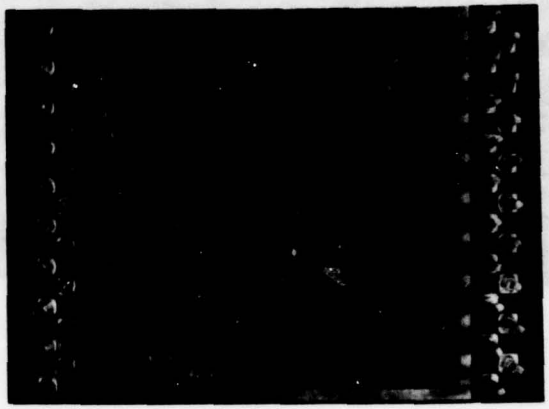
Figure 49. Excised Chips with Their Leads as Used for Assembly; (Top) MMI 5086, (Bottom) Fairchild 93S16.

(a) Lead-Indium Paste Solder Dispensed on Die Bond Pads.

(b) Chips Placed, Aligned, and Fixed in Position for Die Bonding by Solder Reflow.



(c) Die Attach Completed. Solder Placed Over Outer Leads and Bond Pads for Reflow.



(d) Completed Assembly Prior to Cleaning.

Figure 50. Memory Module Hybrid Assembly Sequence.

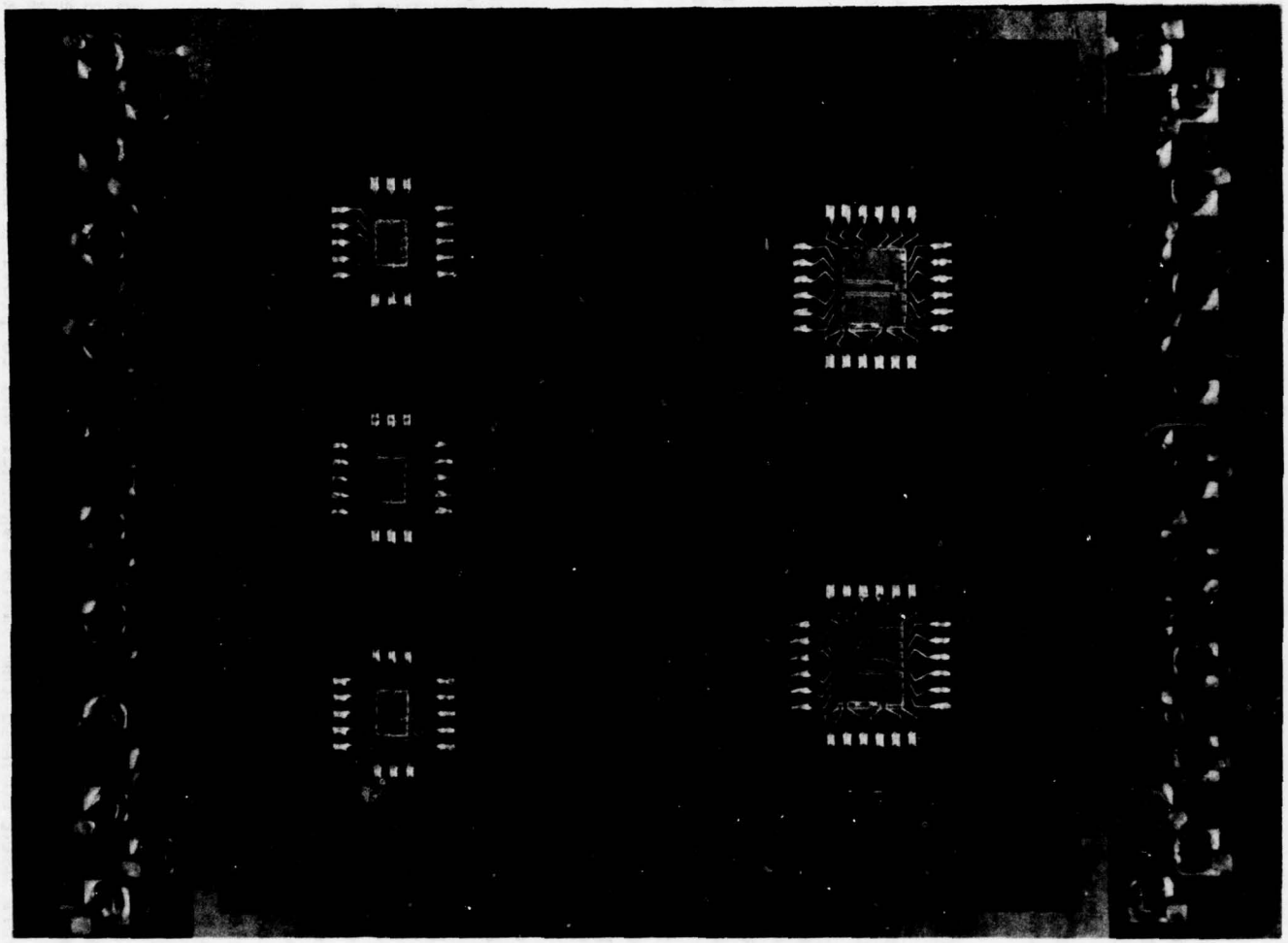


Figure 51. Completed Memory Module Hybrid Assembly.

a group of the resulting outer lead bonds is seen in Figure 52. This hybrid assembly technique was proven successful by the subsequent verification testing.

In those cases where functional testing disclosed defective chips, a similar procedure was used for chip replacement in the hybrid assemblies. The substrate assembly was placed on the hot plate to melt the solder. While the solder was molten, the defective chip was removed using tweezers. After cooling, the bonding pads were scraped lightly with a small dental chisel, thus removing most of the old solder. New solder was applied and the same procedure was used as in the initial assembly. On one substrate, a chip was replaced three times without adversely affecting the remaining ones.

6. Package Sealing

The hybrid package was designed to have a 0.025-inch-thick gold-plated Kovar cover, reflow-solder sealed to the ceramic seal rim with an 80% gold/ 20% tin solder preform, as shown in the substrate cross section of Figure 36. The hermetic sealing operation would be performed with a Solid State Equipment Corporation parallel seam-sealing system. This popular sealing equipment employs opposed rolling electrodes as shown in Figure 53. The mated parts to be sealed are moved beneath the electrodes. A pulsed electrical current is periodically passed through the parts as they roll by, as shown schematically in Figure 54. Local heating is produced within the mating parts to cause either a weld to be formed or to cause the reflow of a solder preform. The package is first moved along the length of one axis, turned 90°, then moved along the second axis to complete the seal.

The rolling electrodes are normally of a relatively small diameter, since packages sealed with this method generally are quite flat. The presence of the 0.400-inch-tall connecting pins on the hybrid package prevented using the available small electrodes. Large diameter electrodes were not available from the equipment vendor. Bar stock from which to make larger electrodes could be obtained from another supplier, but only in 500 pound lots. Consequently, it was decided to seek an alternate sealing method as an expedient to serve the limited quantity immediate needs of the hybrid program. The originally contemplated solder reflow seal still is considered essential to the long-term goals of the hybrid packaging program. Some compromise will be required, however, between the configuration of the connection pins and the size of available sealing electrodes.

Epoxy package sealing was selected instead of the planned reflow solder method. A glass-fabric-supported epoxy film was used, Ablefilm 550-1. Preforms of the film were hand cut to the size of the substrate seal ring. A preform was placed on the raised rim of the substrate and a cover placed on the preform. Figure 55(a) shows these parts. After alignment. spring paper clips were used to hold the parts together and to provide adequate squeeze on the seal area, as shown in Figure 55(b). The assembly then was placed in a vacuum oven which was preheated to 100° C. Then the oven was evacuated to 28 inches of mercury. After a 15-minute vacuum bake to remove any moisture,

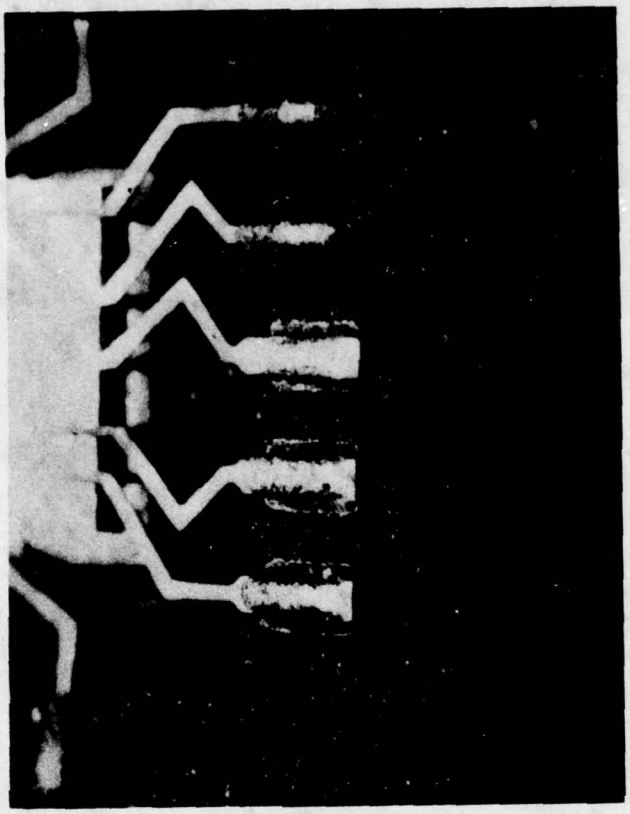


Figure 52. Lead-Indium Solder Reflow Outer Lead Bonds.

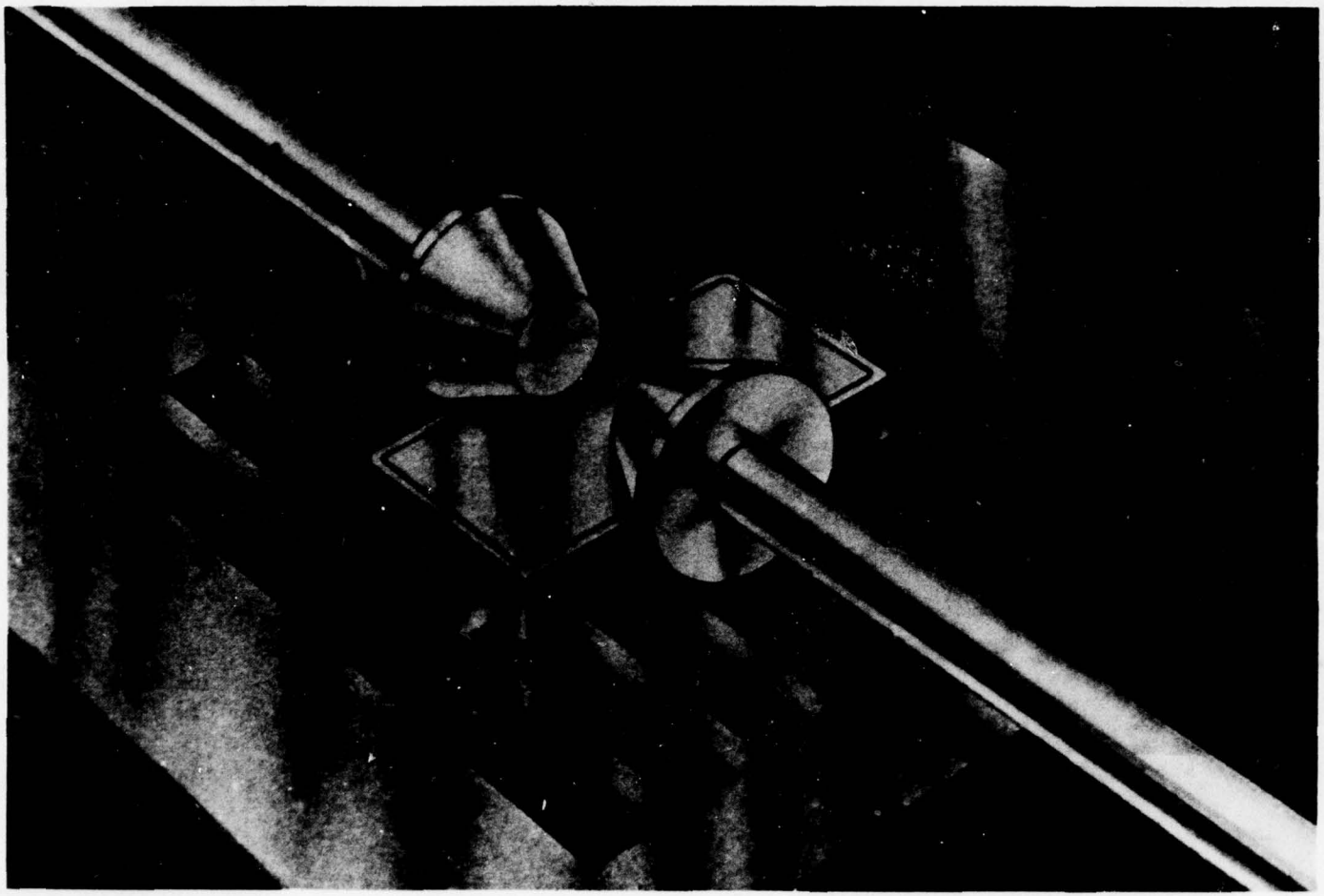


Figure 53. Schematic Showing Parallel Seam Sealing Approach.

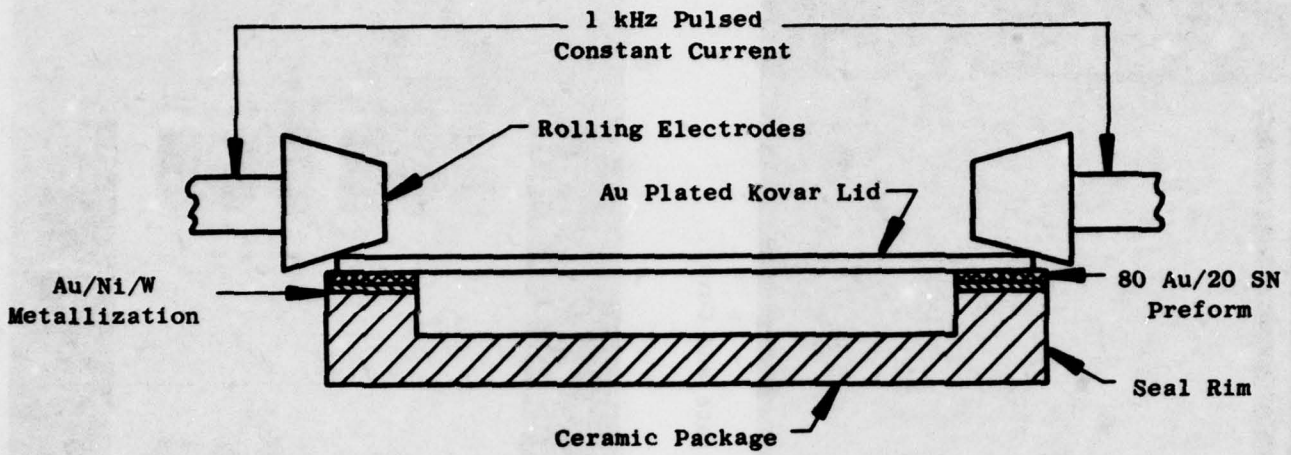
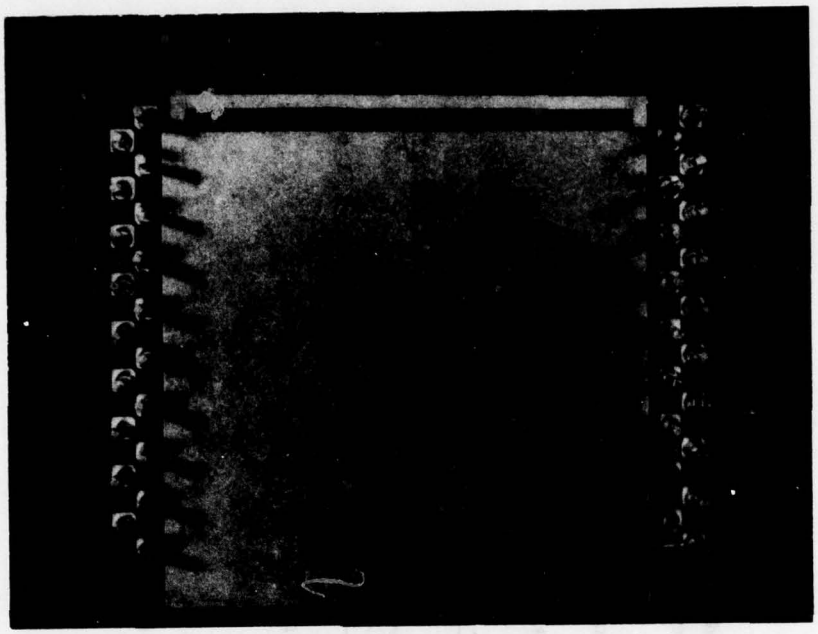
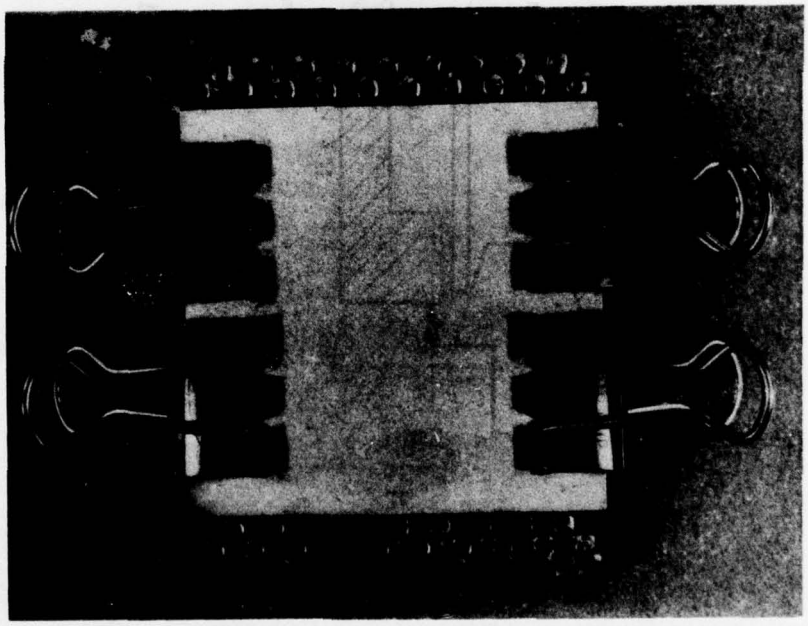


Figure 54. Parallel Seam Reflow Sealing Using an 80% Gold/20% Tin Preform.



(a) Populated Substrate and Cover.



(b) Method Used for Clamping Parts.

Figure 55. Epoxy Package Sealing.

the oven was backfilled with high purity dry nitrogen to a positive pressure of 1/2 psig. Then, the temperature was raised to 150° C and maintained for two hours to cure the epoxy film. The assemblies were removed from the oven. The epoxy seals were inspected and found to be well formed with an excellent wetting of the epoxy to both the metal cover and the ceramic.

Thermal shock cycling was performed on two epoxy-sealed packages. The temperature cycle used was a 30-minute soak at -55° C and a 30-minute soak at +125° C, in air, with a 1-minute transition time between the temperature extremes. The package seals were given a careful visual inspection periodically for any indication of change or failure. The test was conducted for a total of 3000 successful temperature cycles with the absense of any noticeable visible change in the epoxy seal. This testing indicated the suitability of epoxy sealing to the immediate short-term need of the packaging program but does not necessarily recommend it to longer term field-service needs.

SECTION IV

MOUNTING, INTERCONNECTION, AND HEAT TRANSFER

1. Direct Mounting To An Aluminum Bracket

The hybrid assembly mounting and interconnection concept is shown by Figure 56. Maintainability, mechanical integrity, and heat transfer were the major factors considered in the concept selection. The chips are mounted to the front side of the alumina circuit board or substrate and then covered. The interconnection pins also project from the front side of the substrate so that the back side of the substrate is flat. Interconnections between hybrid assemblies and connectors are made by wire wrapping and soldering leads to the pins. These connections then are potted with RTV for mechanical support and damping. Figure 57 shows a section of a control using the above concept.

In regards to heat transfer, the back side of the hybrid assembly was loaded against a flat surface on the aluminum mounting bracket by the spring-type retaining clips. The mounting bracket, in turn, was bolted to the chassis bottom. The resulting heat transfer path is from the chip through the thickness of the alumina substrate to the aluminum bracket, then down the bracket to the fuel-cooled chassis bottom. The alumnia substrates were lapped flat, and a thermally conductive, electrically insulative grease was used to maximize the heat transfer across the substrate/bracket interface. This provided low thermal resistance which is important for high-density hybrid packaging.

Estimates were made on the temperature drop (ΔT) required to transfer one watt and two watts per square inch from the chip to the fuel coolant. The results are shown in Figure 58. With a two-inch bracket height and an average substrate heat density of 1 watt per square inch, the maximum calculated ΔT is 17.5° F between a high power LSI memory chip and the fuel.

2. Alternate Mounting Arrangements

A second approach, also shown in Figure 58, is recommended for heat densities above two watts per square inch or for bracket heights greater than two inches and for supersonic aircraft engine applications. The hybrid boards are loaded against an aluminum sandwich structure through which fuel passes. The heat path is from the chip, through the alumina substrate thickness, through the aluminum plate thickness, through the tube wall, and into the fuel. For the analysis, the flatness of the sandwich structure and the hybrid substrate were controlled and a thermally conductive grease was used to minimize the ΔT developed across the substrate/aluminum-plate interface. The maximum ΔT incurred between a high power LSI chip and the fuel by a peak substrate heat density of four watts per square inch is approximately 10° F if the tube were located directly under the chip. Appendix C provides additional data on heat transfer analytical results.

The third approach shown in Figure 58 is similar to the second except that air was used as the cooling media. This approach is satisfactory for

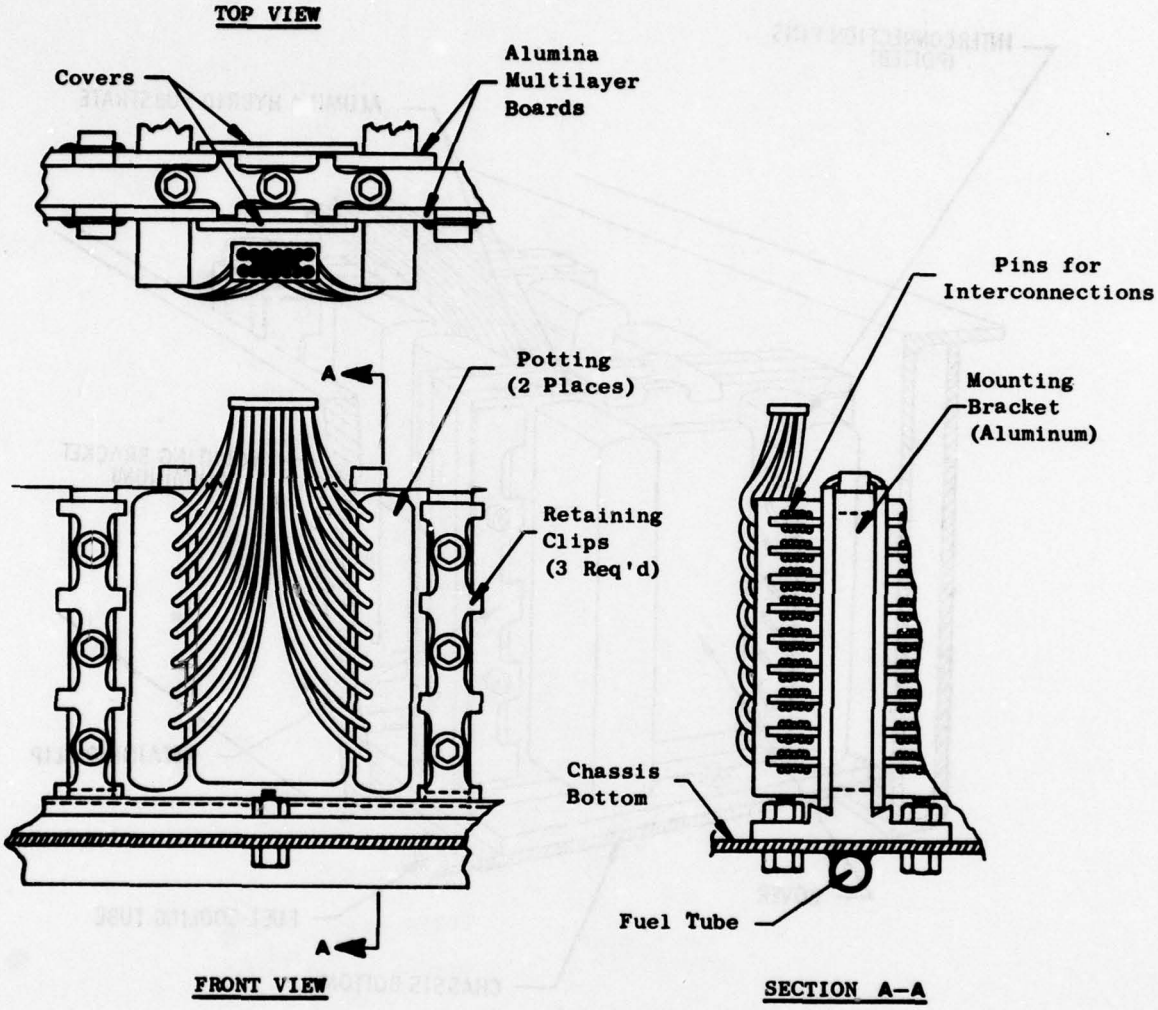


Figure 56. Mounting and Interconnection Concept.

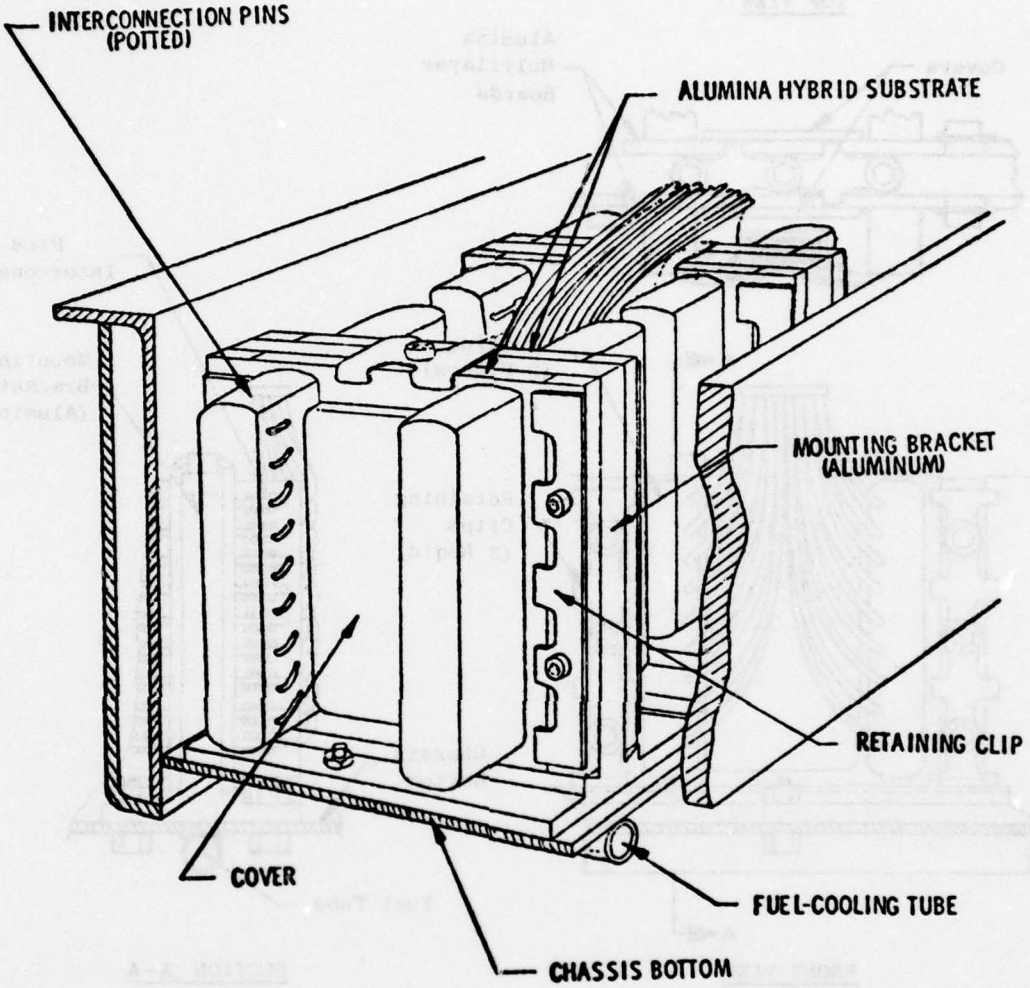
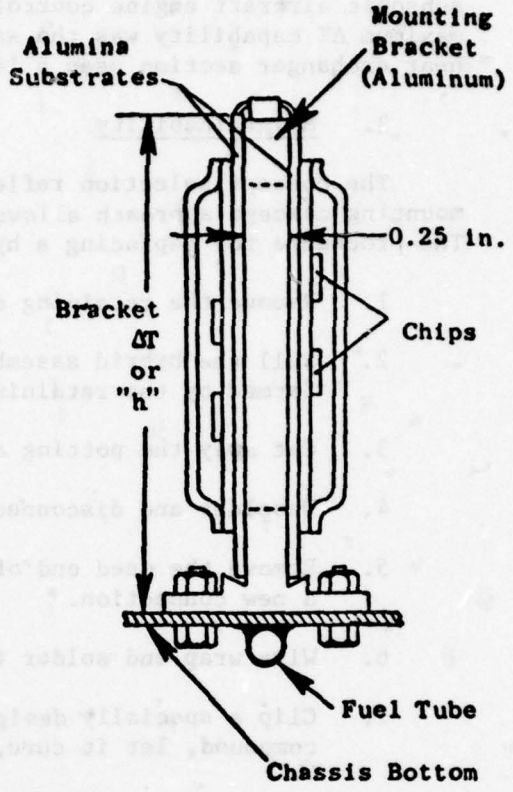
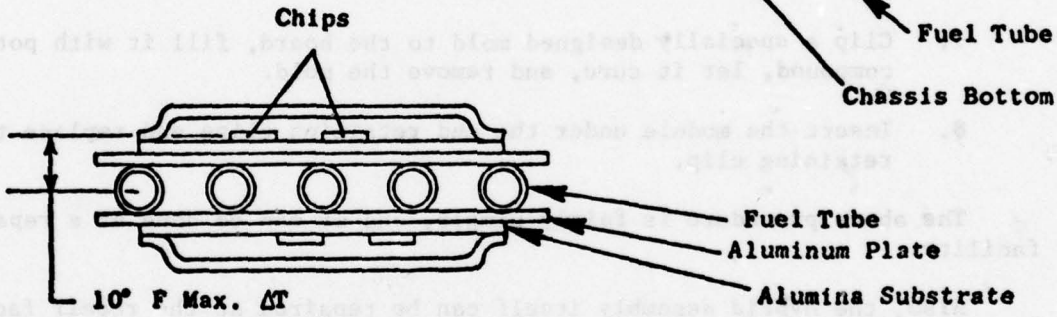


Figure 57. Electrical Control Cross Section Showing Hybrid Assembly Mounting Concept.

Average* watts/in.^{2}	h (in.)	Bracket ΔT (° F)	Max. ΔT* Coolant to Chip (° F)
1	2	7.5	17.5
2	2	15	25
1	3	17	27
2	3	34	44

*Each Side





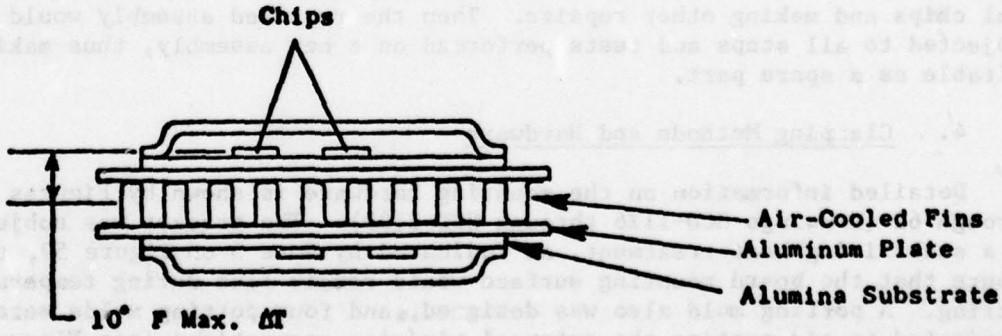


Figure 58. Heat Transfer Comparisons.

subsonic aircraft engine controls, such as those used on helicopters. The maximum ΔT capability was the same as that for fuel cooling, because the air heat exchanger section uses a large heat-transfer fin area.

3. Maintainability

The concept selection reflects maintainability considerations. The mounting concept approach allows easy replacement of a part of the control. The procedure for replacing a hybrid assembly (see Figure 56) is as follows:

1. Remove the retaining clip at the top of the mounting bracket.
2. Pull the hybrid assemby up, and it will slide out of the slot formed by the retaining clips and the bracket.
3. Cut away the potting around the connections.
4. Unsolder and disconnect the leads.
5. Remove the used end of the wire, and strip a length sufficient for a new connection.
6. Wire wrap and solder the leads to pins on a new hybrid assembly.
7. Clip a specially designed mold to the board, fill it with potting compound, let it cure, and remove the mold.
8. Insert the module under the end retaining clips and replace the top retaining clip.

The above procedure is fairly simple, and it can be done at a repair facility.

Also, the hybrid assembly itself can be repaired at the repair facility. Techniques exist for removing the cover - this permits replacing the individual chips and making other repairs. Then the repaired assembly would be subjected to all steps and tests performed on a new assembly, thus making it suitable as a spare part.

4. Clamping Methods and Hardware

Detailed information on the mounting hardware is shown by Figures 59 through 62 (Drawings HCD-1126 through HCD-1129). The bracket was subjected to a stabilizing heat treatment, as indicated by Note 5 on Figure 59, to assure that the board mounting surface would remain flat during temperature cycling. A potting mold also was designed, and four potting molds were fabricated to aid potting the external pin/wire connections (see Figure 63 or Drawing HCD-1125).

The end board retainer, top board retainer, and shim (Figures 60 through 62) are used in the clamping arrangement shown in Figure 56. The end board

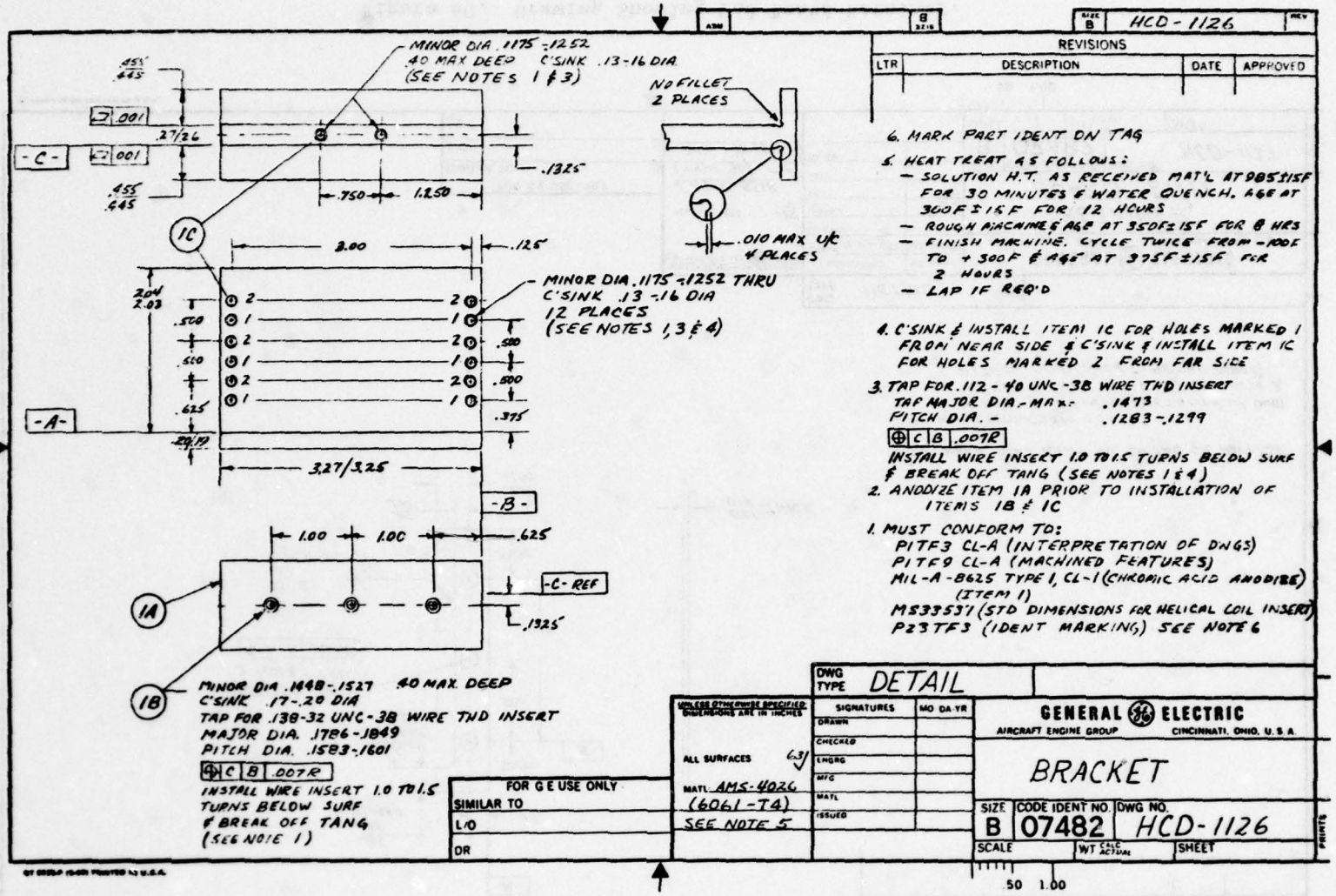


Figure 59. Drawing Showing Aluminum Mounting Bracket.

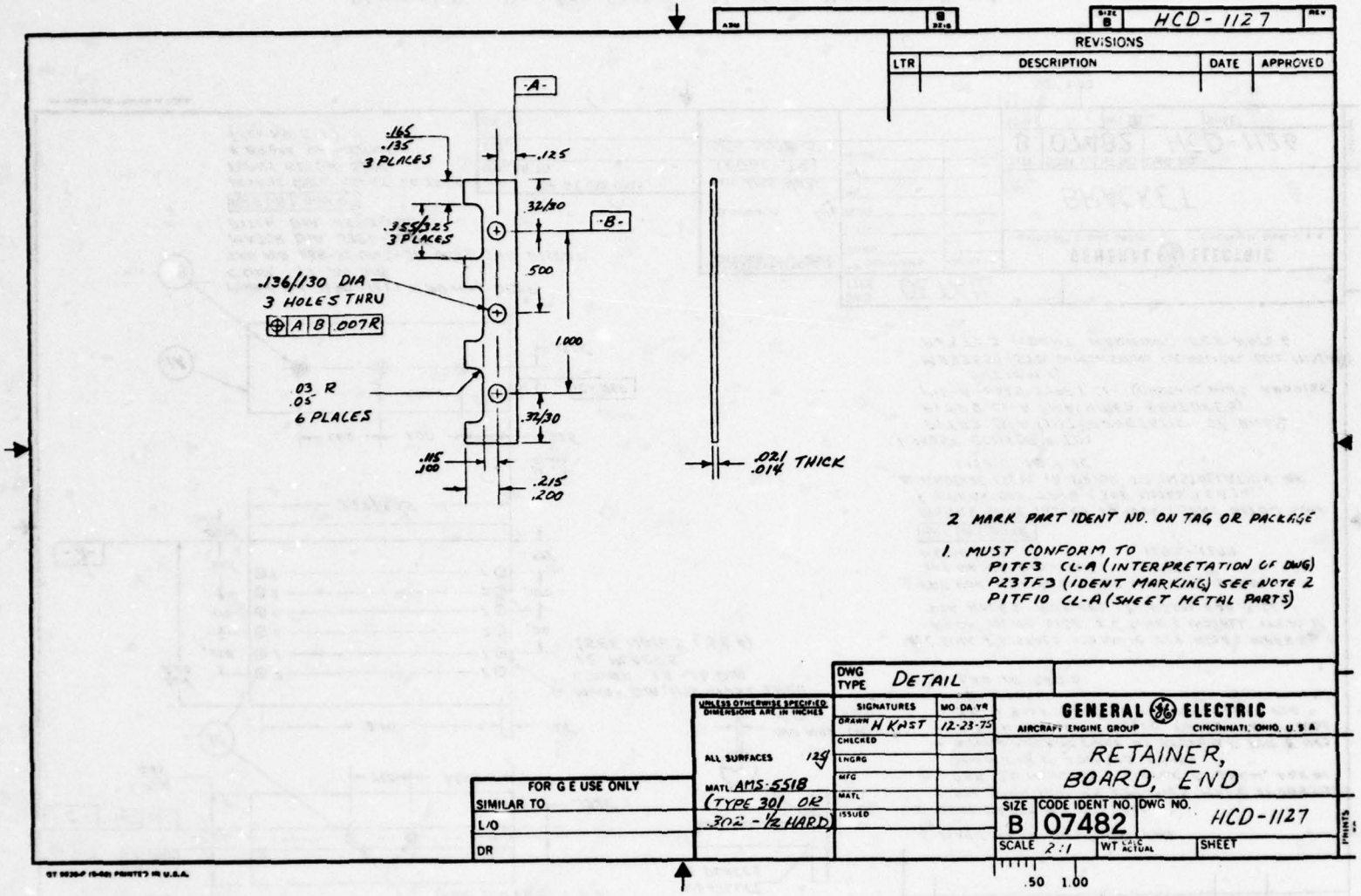


Figure 60. Drawing Showing End Board Retainer.

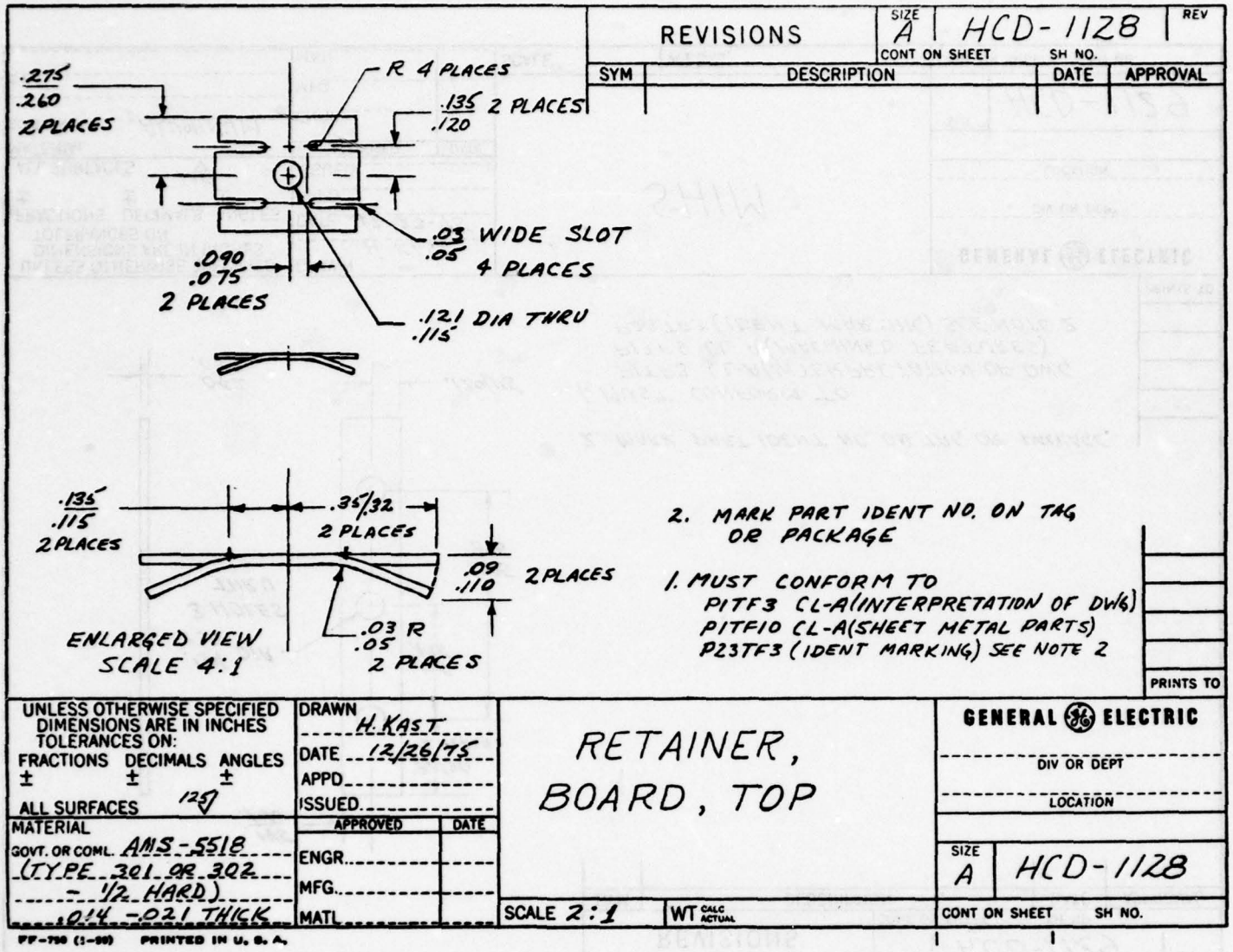


Figure 61. Drawing Showing Top Board Retainer.

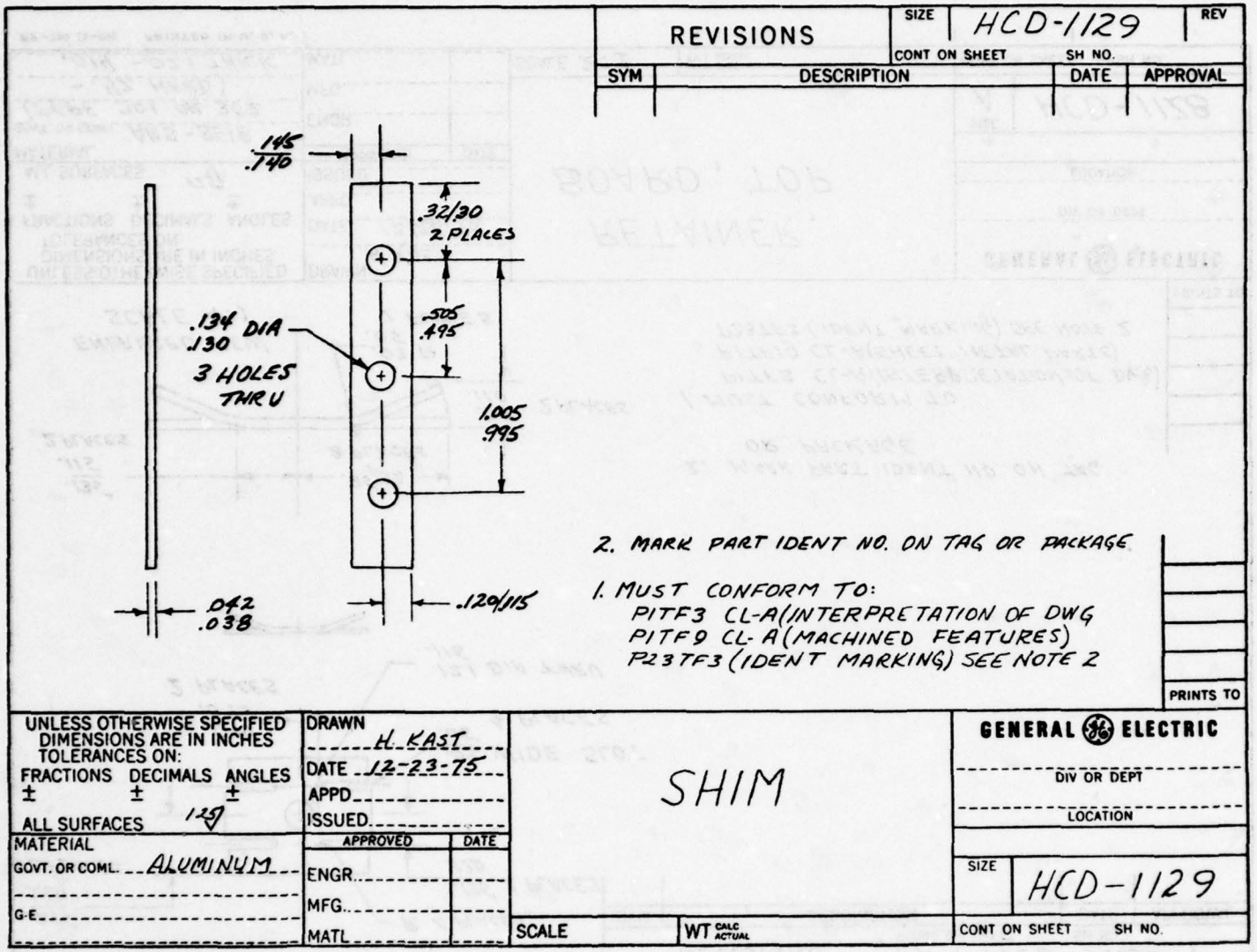


Figure 62. Drawing Showing Shim.

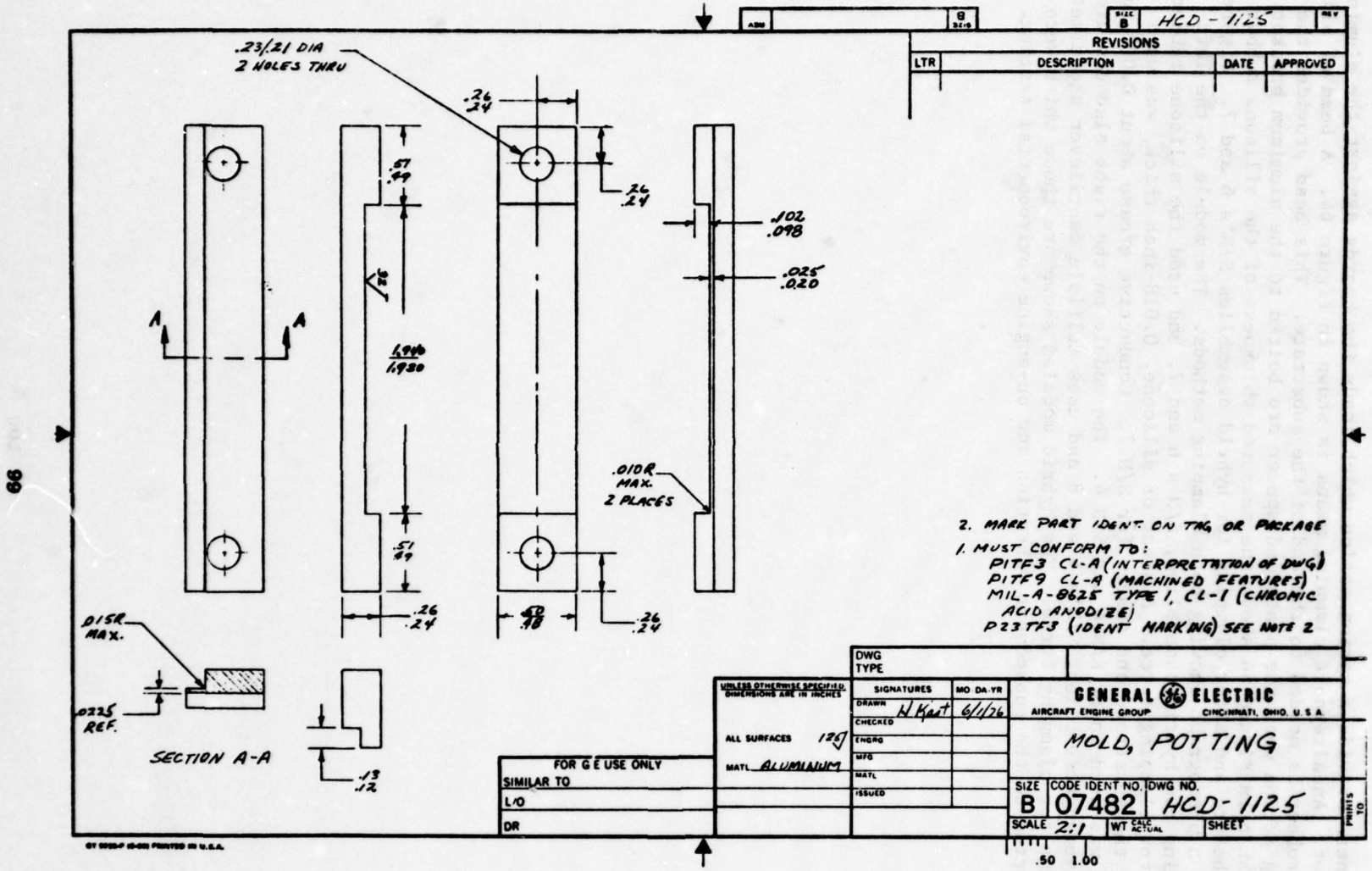
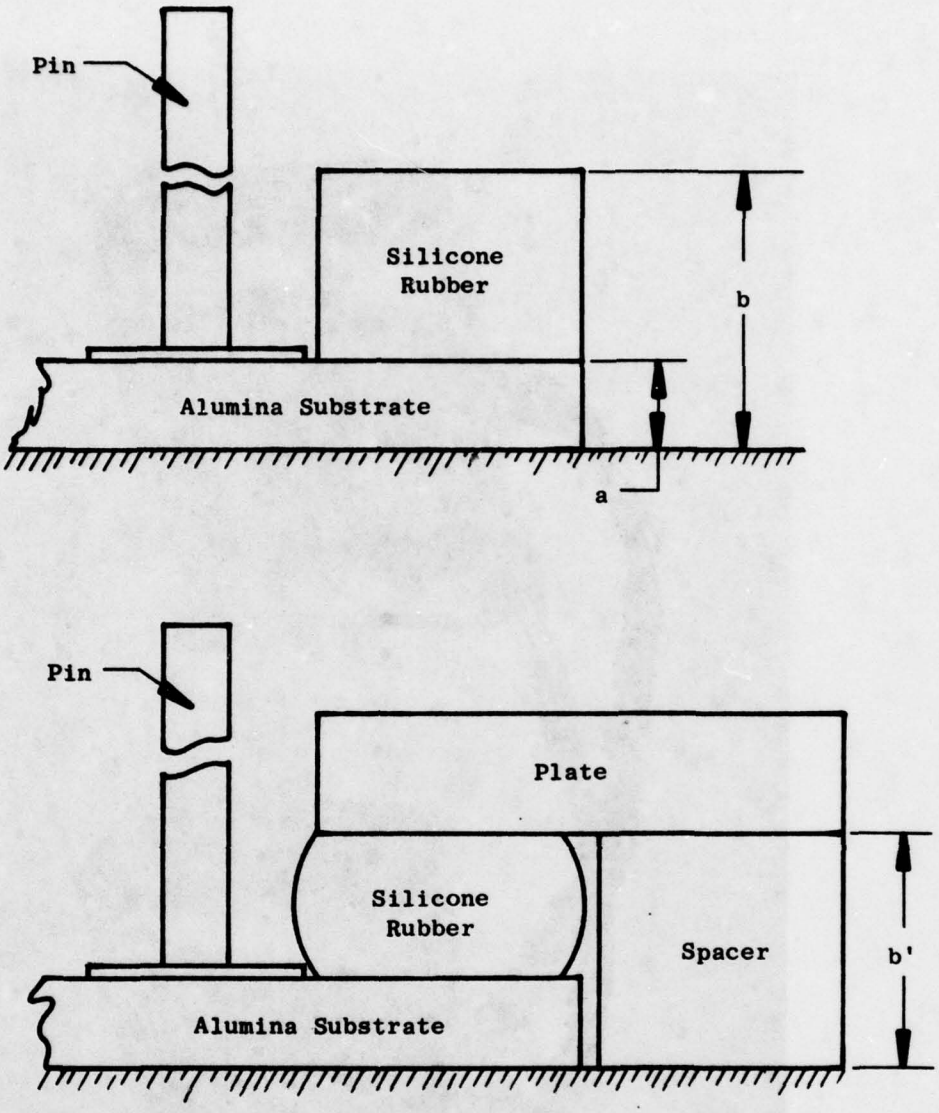


Figure 63. Drawing Showing Potting Mold.

retainers provide a spring action which loads the boards against the aluminum bracket. An alternate clamping means is shown in Figure 64. A bead of silicone rubber is molded to the end of the substrate. This bead provides the spring action when the plate and spacer are bolted to the aluminum bracket. The table in Figure 64 shows the measured thickness of the silicone rubber bead before and after clamping for hybrid assemblies S/N's 6 and 7. Figure 65 is a photograph showing both clamping methods. The module on the left contains two hybrid assemblies, S/N's 6 and 7, and used the silicone rubber bead for clamping force. A sheet of silicone, 0.018-inch thick, was used under the substrate and spacer for S/N 7. Conductive grease about 0.002-inch thick was used under S/N 6 and S/N 4. The module on the right also contains two hybrid assemblies, S/N's 4 and 8 and uses multiple cantilever sheet metal springs for clamping force. The hybrid modules shown are those which were subjected to the subsequent vibration and on-engine environmental testing.



Assembly	a	b	b'
S/N 6	0.050	0.160	0.137
S/N 7	0.048	0.170	0.137

Figure 64. Alternate Clamping Method Using Silicone Rubber Beads.

Figure 65. Hybrid Modules Showing Two Clamping Methods.

SECTION V

TESTS

1. Temperature Cycling, CII Honeywell Bull Hybrids

About midway through the program, while still in the design phase for program hardware, the need was recognized for information on the behavior of TAB-bonded silicon devices under exposure to repeated temperature cycling. Such information then was unavailable. As a way to obtain such information first hand, an arrangement was made to have CII Honeywell Bull (CII HB) build some TAB-equipped substrates for General Electric to temperature test. These substrates were fabricated completely by CII HB using their established processes.

Two groups of five assembled substrates were obtained, differing only in the die attach and outer lead bonding materials. One side of the 1×2 inch alumina substrate provided a thick-film multilayer interconnection pattern for four TAB-assembled integrated circuit chips. There were two screen-printed layers of gold conductor patterns isolated by an intervening layer of screen-printed thick-film dilectric. The interconnection pattern provided electrical access to all connections of the integrated circuits by means of connecting pads along two edges of the substrate. A substrate assembly is shown in Figure 66. An individual TAB-bonded chip is seen in Figure 67.

Each substrate was assembled with four Fairchild 74S04 hex inverter chips. These are industrial grade, rated to operate over a 0° to 70° C temperature range. Each chip provides six independent transitor-transitor-logic (TTL) inverter circuits whose output is simply the inverted polarity of the input logic signal. An assembly thus contains a total of 24 testable logic functions. The chips were obtained from Fairchild complete with BETA-processed gold bumps and silicon dioxide passivation. Inner lead bonding was done by CII HB to tin-plated copper TAB tapes with a gold-tin fusion bond.

The two substrate groups were identified by the materials used for bonding as follows:

Group	Outer lead Bond	Die attach
E	50% Lead/50% Indium Solder	Epoxy
S	80% Gold/20% Tin Solder	50% Lead/50% Indium Solder

A thermally conductive, electrically insulating epoxy, Elocolit 601, was used for die attach for the Group E substrates. The solders were applied to the substrates in paste solder form. The assemblies were not sealed.

Both groups of substrates were given a thorough dynamic electrical test at room temperature prior to being subjected to temperature cycling. Each

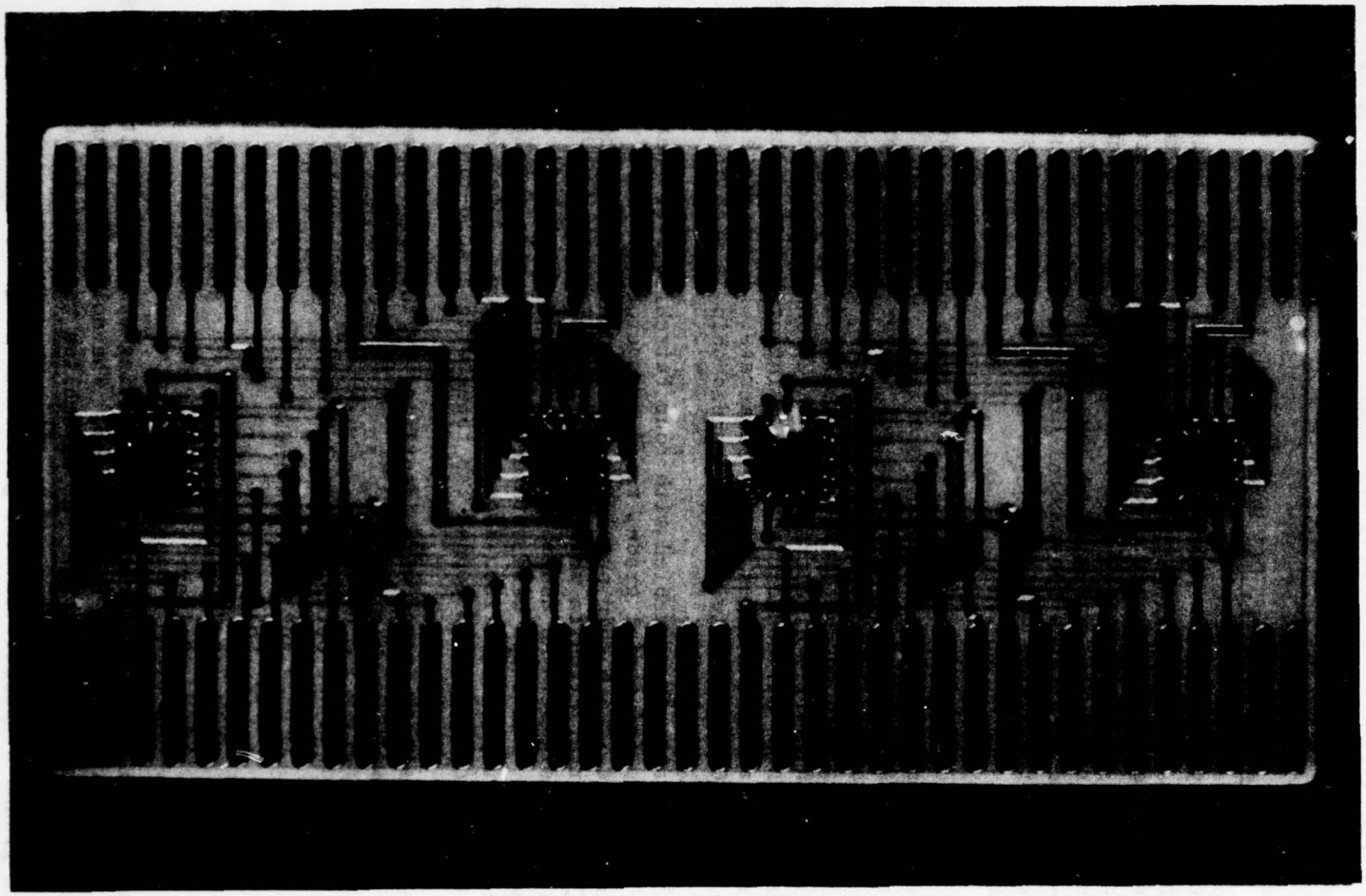


Figure 66. A CII Honeywell Bull TAB Test Substrate Used for Thermal Shock Temperature Cycling.

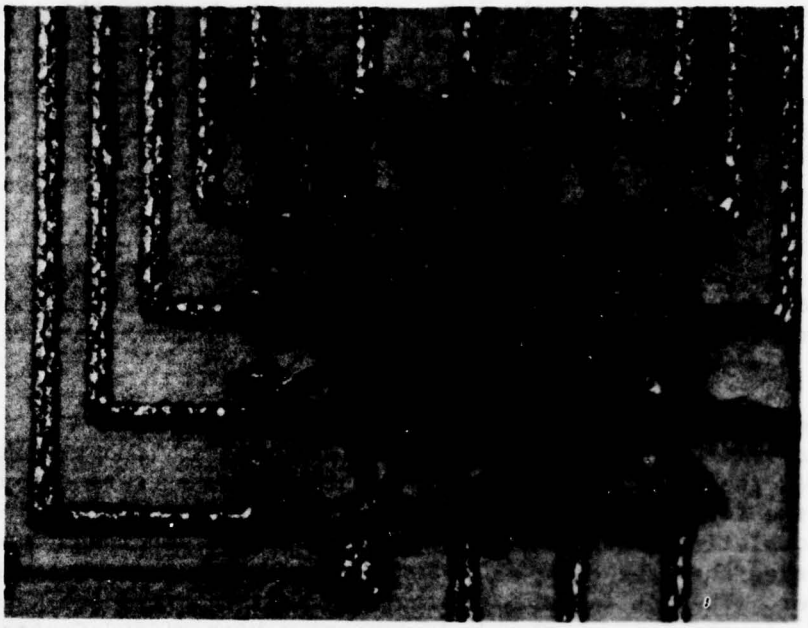


Figure 67. An Individual TAB-Bonded Chip on a TAB Test Substrate. This Chip was Bonded Using Epoxy.

substrate contains 24 testable electrical functions for a total of 120 functions in each group. They they were placed in a temperature cycling test chamber. The temperature cycle was a 20-minute soak at -55° C alternated with a 20-minute soak at +125° C, in air, with a 1-minute transition time between the temperature extremes. Periodically, the substrates were removed from the chamber, while hot, and tested electrically at room temperature. They then received a detailed visual inspection with magnifications as high as 70× before return to the chamber for a continuation of the temperature cycling.

The equipment used was a Tenney Model T5TS-100350 thermal shock chamber. It consists of a lower mechanically refrigerated cold chamber coupled to an upper electrically heated hot chamber. A hydraulically actuated test specimen basket is provided that alternately transfers between the two chambers. The basket is constructed to seal the opening between the hot and cold chambers when it has fully entered either one of the chambers. Later, peculiarities in the performance of this equipment were found to have a significant influence on the temperature cycling results of the TAB test substrates. This testing was the first use of a new piece of equipment and its limitations were not yet understood.

As the temperature cycling progressed, the substrates were tested and inspected after 10, 25, 50, 100, 200, and 500 cycles without change. During this period, the control for the chamber had been preset to automatically terminate the test and to shut down the equipment upon the completion of 1000 cycles. Completion occurred late one Friday night. On Monday morning, it was discovered that the equipment had shut down with the substrates in the cold chamber. The continuously monitoring chart recorder indicated that the temperature in the cold chamber had risen to a high of 50° C after shutdown. Also a large amount of water was found in the cold chamber, produced by the melting of frost which had accumulated during the operating period on the refrigeration evaporator within the cold chamber. Thus, it was realized that the test substrates had been subjected to an unintentional prolonged exposure to very high humidity at a temperature as high as 50° C. The exposure time was about 36 hours, as read from the chart recorder.

Testing of the substrates after 1000 temperature cycles and the accidental humidity exposure disclosed the failure of one logic function on one of the epoxy-bonded Group E substrates. This substrate was withdrawn from further testing for a failure analysis study, the results of which are discussed later. The remainder of the substrates were returned to the chamber to continue temperature cycling. Tests and inspection after 1500 and 2500 cycles continued to be satisfactory.

At 3185 cycles, the refrigeration system failed because there was an insufficient charge of refrigerant, again on a Friday night. Once more the frost melted, creating another high humidity condition of a weekend duration. However, the elevator continued to cycle so that the exposure of the substrates to the humidity was not as drastic as after the 1000-cycle shutdown. The refrigeration system was recharged on Monday, and the chamber resumed operation. The substrates were tested, inspected, and returned to temperature cycling.

Again, at 5000 cycles, an unanticipated automatic shutdown of the equipment occurred, once more exposing the substrates to high humidity, but only overnight. They were tested and inspected once more. Now failures were found on two Group E substrates. One was a single logic function failure, the other was the failure of an entire chip containing six logic functions. There were no failures through 5000 cycles in the completely solder-bonded Group S substrates. By contrast, there was a cumulative total of eight logic function failures in the epoxy-bonded Group E substrates. At that point, it was decided to terminate the temperature cycling of the TAB test substrates.

Visual inspection of the substrates after 5000 temperature cycles revealed a subtle change in the appearance of the TAB lead surfaces. Early in the cycling, the appearance of the tin plating slowly changed from bright metallic through dull light grey to dull dark grey. This was accepted as the slow oxidation of the tin associated with continued exposure in air to the 125° C temperature. But now, in addition, the leads had a very slight green coloration. It was some time before this coloration could be understood.

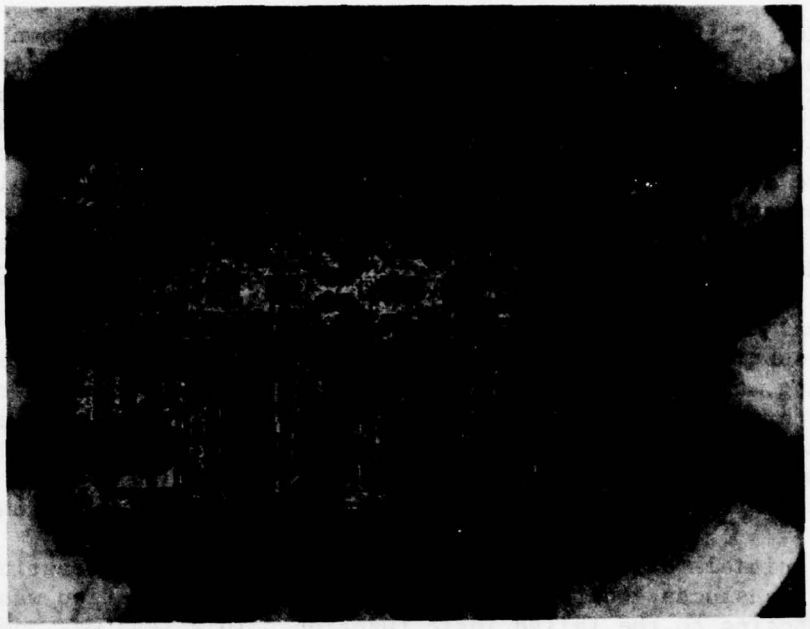
The initial failure of the Group E substrate was interesting because a foreign, translucent-white (almost crystalline) encrustation was found on the lead connecting to the failed logic function. This lead was open circuited at the chip. Also, a trace of similar appearing material was found on an adjacent lead, but nowhere else on the chip. Figure 68(a) shows the chip and 68(b) shows the affected leads as seen initially with a light microscope.

A Cambridge Model S4 scanning electron microscope (SEM) was used to study the failure. This microscope is equipped with an energy-dispersive X-ray spectrometer (EDX) and a wavelength-dispersive spectrometer (WDX) for surveying and identifying elements down to boron. Figure 69(a) is a SEM view of the failed chip. The involved lead is the middle one in Figure 69(b) and is shown in Figure 69(c) enlarged. The encrustation of the lead can be seen to have two distinct components. The upper surface has attached to it a mass of small particles, while the sides are encased in an amorphous material suggestive of "dried mud."

EDX element maps of chlorine, aluminum, copper, silicon, and tin are shown, respectively, in Figure 69(d) and in Figure 70(a-d). These element maps correspond to Figure 69(b). A comparison of the maps with the topographic view produces some interesting observations:

1. Chlorine is strong on the copper leads and in the corrosion zone on the chip. The concentration is extraordinarily high for the known process history of the assembly.

2. Some aluminum has been transported to the top of the lead [Figure 70(a)], and copper has been displaced to the right of the lead [Figure 70(b)] This strongly suggests that a galvanic transport mechanism was involved, with copper and aluminum together and in the presence of water and chlorine.



(a) A View of the Failed Chip.

(b) An Encrustation on the Failed Lead.

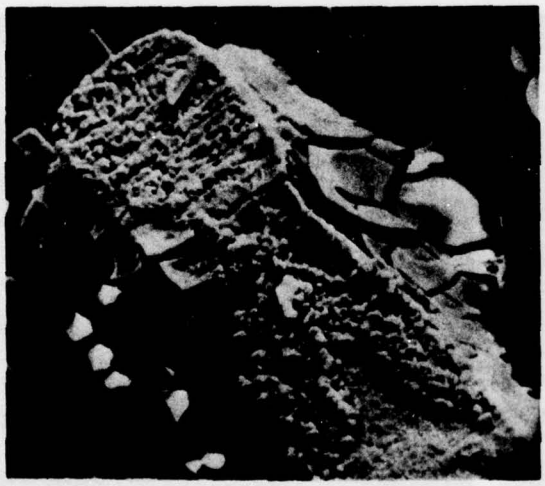
Figure 68. The First Epoxy-Bonded Chip Failed After 1000 Cycles.

No. 2 50X

(a) SEM View of the Failed Chip.

No. 2 210X

(b) SEM View of the Involved Leads.



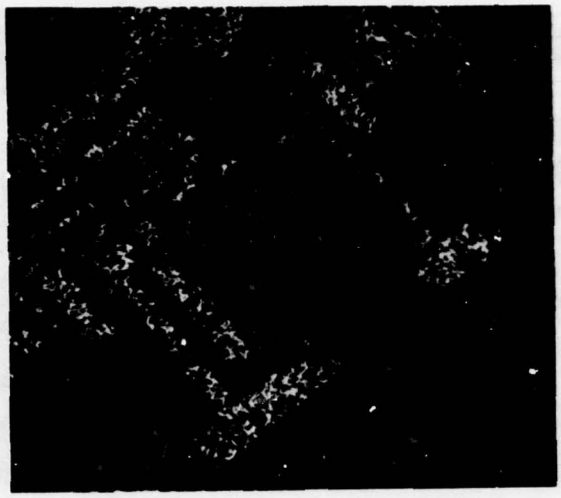
No. 2 500X

(c) SEM View of the Failed Lead Showing the Encrustation.

Cl 210X

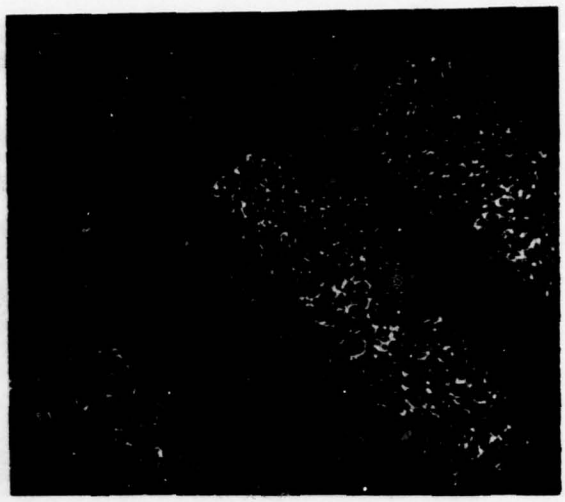
(d) Elemental Map Showing Strong Presence of Chlorine on the Leads.

Figure 69. Failure Analysis Evidence - 1.



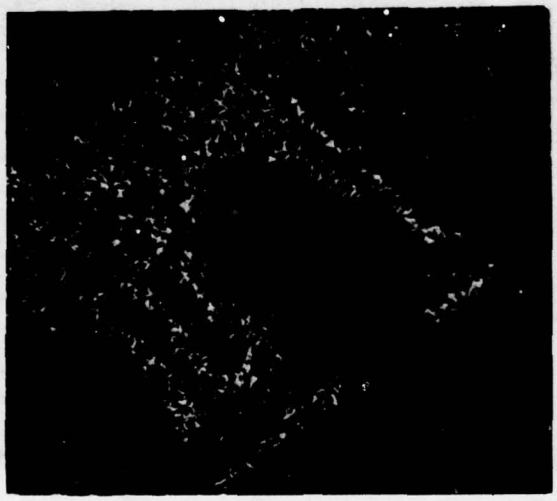
Al 210X

(a) Elemental Map of Aluminum.



Cu 210X

(b) Elemental Map of Copper.



Si 210X

(c) Elemental Map of Silicon.

Sn 210X

(d) Elemental Map of Tin.

Figure 70. Failure Analysis Evidence - 2.

3. Past experience with other analyses by electron diffraction methods has identified the "dried mud" appearance of the corrosion product as characteristic of hydrated aluminum oxide formed by a chlorine attack on native aluminum oxide in the presence of water.

The probable cause of this failure in the connection was defined as galvanic attack of the aluminum pad on the chip in the presence of water and a strong concentration of chlorine. There may have been a defect in the silicon oxide passivation near the involved pad, the defect providing an opening which exposed the pad to attack, since elsewhere the aluminum was undisturbed. The remaining mystery was the source of both the chlorine and the water.

The now strong evidence of chlorine from some still unknown source suddenly became significant in explaining the coloration imparted to the copper TAB leads after 5000 temperature cycles - the formation of copper chloride. At first, the chlorine was thought to be a residue of a cleaning operation, but its concentration was too strong. Eventually, suspicion was cast upon the atmosphere within the temperature chamber. A sample of frost was collected from the evaporator in the cold chamber and analyzed by X-ray emission spectrography (XES). The result was a strong concentration of chlorine in the frost and, hence, whithin the temperature chamber itself.

Ultimately, the source of chlorine was traced to a minute leak in the refrigeration system, between the inner and outer walls of the chamber, which allowed some of the R-13 refrigerant to enter the inner chambers. It was this refrigerant leak that caused the chamber to fail after 3185 cycles. Once inside the inner chambers, the refrigerant was circulated over the heating coils. The heat partially decomposed the chlorofluorocarbon refrigerant to release free chlorine which also circulated within the chambers, tending to concentrate in the frost on the evaporator. Once found, the leak was repaired and, thereafter, a continuous purge of dry, high-purity nitrogen was used in the chamber during all temperature cycling. The purge greatly reduces the frost buildup on the evaporator.

Subsequent use of the chamber disclosed another unusual phenomena. Besides forming on the evaporator coils, frost has been observed on the blade tips of the fan which blows the circulating air through the evaporator. Occasionally, small particles of frost have been seen to break free from the fan. Then these frost particles are carried by the air stream, through the evaporator, and into the cold chamber. It is quite possible that one or more of these frost particles could have landed on the unprotected TAB test substrates. Later, when melted in the heated chamber, the resulting droplet of chlorine-contaminated water could initiate the failure mechanism described above.

It is truly remarkable that the TAB test substrates performed so well. Besides thermal shock temperature cycling, there was the unintentional exposure to severe humidity conditions in a hostile, chlorine-contaminated environment. There was no observable deterioration attributable to the

thermal cycling. The changes which did occur resulted from wet chemical contamination which would be avoided in a normal hybrid operating environment. This potential problem was avoided by sealing the assemblies fabricated for this program.

There were no failures in the solder-bonded Group S substrates despite the use of unprotected silicon chips in the hostile environment. The total of eight function failures on the epoxy-bonded Group E substrates suggests that the presence of the epoxy may have affected test survival adversely.

2. Thermal Shock Cycling of Program Hybrid Assemblies

Two of the earliest assembled substrates, uncovered and populated with nonoperating TAB-mounted semiconductor chips, were subjected to thermal shock temperature cycling. The procedure used was similar to that for the TAB test substrates described earlier in Section V.1. Now, the test chamber was functioning properly; furthermore, it was continuously purged with nitrogen as a precautionary measure. The temperature cycle was a 30-minute soak at -55° C alternated with a 30-minute soak at +125° C, in nitrogen, with a 1-minute transition between the temperature extremes.

Periodically, the assemblies were removed from the chamber and visually inspected with magnifications as high as 70×. A dental tool was used to carefully probe the TAB leads and bonds at selected sites in search of bond failures. Too few assemblies were available to allow destructive testing. The assemblies were returned to the chamber to resume cycling. This procedure was repeated after 10, 50, 100, 500, 1000, and 2000 cycles.

Thermal shock temperature cycling was terminated after 3000 cycles because no significant change could be found in the assemblies. There was a gradual darkening of both the tin plating and the surface of the lead-indium solder. This discoloration is caused by surface oxidization of the metals and would not have occurred within a sealed package containing a protective atmosphere. No change could be seen in the morphology of the solder. Hence, it is concluded that the assemblies successfully survived 3000 thermal shock cycles without change.

3. Hybrid Module Exerciser

An electrical unit was built to continuously monitor the outputs of the hybrid module (or assembly) circuitry. The unit contains a circuit equivalent to the hybrid module circuit. This is used as a reference, and its outputs are continuously compared with those of the hybrid circuit. If the two outputs disagree, the clock circuit is disabled, a fault indicator lights, and the address lights on the front of the unit displaying the memory location of the fault. The clock circuit in the unit has two speeds. When the module is connected to the unit through a long cable, as would be the case during on-engine testing, the slow speed (388 kilohertz) would be used commensurate with cable rise time limitation. The fast speed (7 megahertz) requires short cables and is used to test the access time of the module memories. The unit contains all the functions necessary to drive and to

exercise the hybrid circuit. Figure 71 is a photograph of the hybrid module exerciser.

4. Functional Testing of Hybrid Assemblies

The hybrid assemblies, constructed at GE R&DC in Schenectady, were functionally tested and evaluated at GE-AEG in Evendale. The first four were tested functionally at room temperature without covers with results as follows:

Serial No. 1 - This assembly had a pin/substrate joint problem. This was the first indication that an improved brazing process was needed. When a ganged connector was attached to the pins, the small force broke several pins from the substrate. The failures occurred at the tungsten/alumina interface. The pin/substrate joint problem and its solution are discussed in Section III.1.

Serial No. 2 - This assembly exhibited proper operation of its internal counter chips. However, one of the internal Read Only Memories (ROM's) had a range of addresses for which its four least significant outputs, D1 to D8, did not meet output voltage requirements for logic circuits. This improper operation can be seen in the two attached photographs, Figures 72 and 73. Figure 72 shows a complete cycle of the memory addresses for the hybrid assembly. The top trace is signal A1024 (Figure 4, Drawing ACE 226 in Section II.3.). Th bottom trace is output D1. A region can be seen on the trace where the output is about half the required value. Figure 73 shows an enlarged view of the improper waveforms. This improper output occurred only when A1024 was low, indicating that the left memory did not meet minimum specifications.

Serial No. 3 - This hybrid assembly had the same pin attachment problem discussed under Serial No. 1.

Serial No. 4 - This assembly showed proper functioning of the counter. However, when signal A1024 was high, the 10 output pins of the assembly were also high. This indicated that the right memory chip was not enabled, implying that there was an "open" somewhere in the A1024 signal line.

Since S/N's 2 and 4 had satisfactory pin/substrate joints, these two assemblies were subjected to a visual examination. These assemblies were examined with the aid of a microscope, and in both cases the problem was identified as a defective MMI memory chip. Both suspect chips were found to contain silicon wafer processing defects. The chip in S/N 2 contained two aluminum etch defects, Figure 74, that prevented electrical contact from aluminum conductor runs to the diffused feed-through connections. The chip in S/N 4 had three adjacent aluminum conductors which appeared to have been shorted together by an amorphous growth within the aluminum, Figure 75. A second growth region also was noted nearby, but it apparently caused no short between conductors. Both assemblies were repaired by replacing a memory chip.

Following this rework, functional test indicated that S/N 4 was satisfactory, while S/N 2 was not. Examination of S/N 2 indicated a broken lead bond. The unusual shape of lead involved suggested accidental handling damage of the uncovered hybrid assembly. The involved memory chip was replaced.

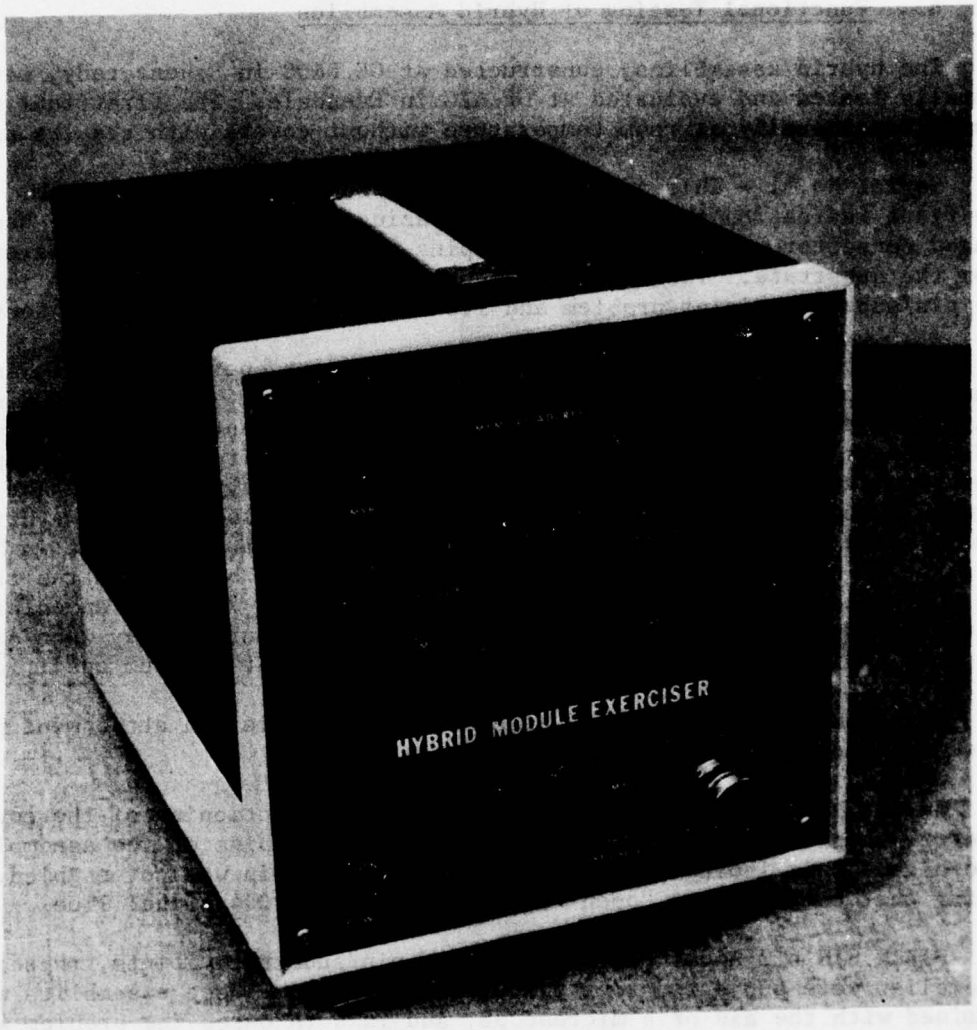


Figure 71. Hybrid Module Exerciser.

Figure 72. Oscilloscope Display of Memory Chip Showing Complete Output Including Range of Improper Operation.

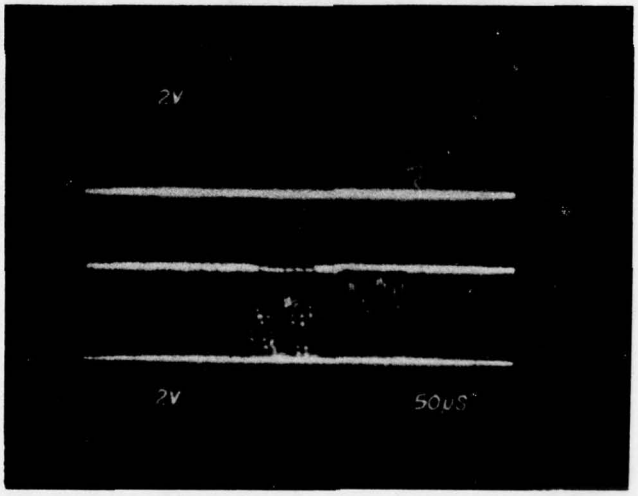


Figure 73. Oscilloscope Display Showing Only Range of Improper Operation.

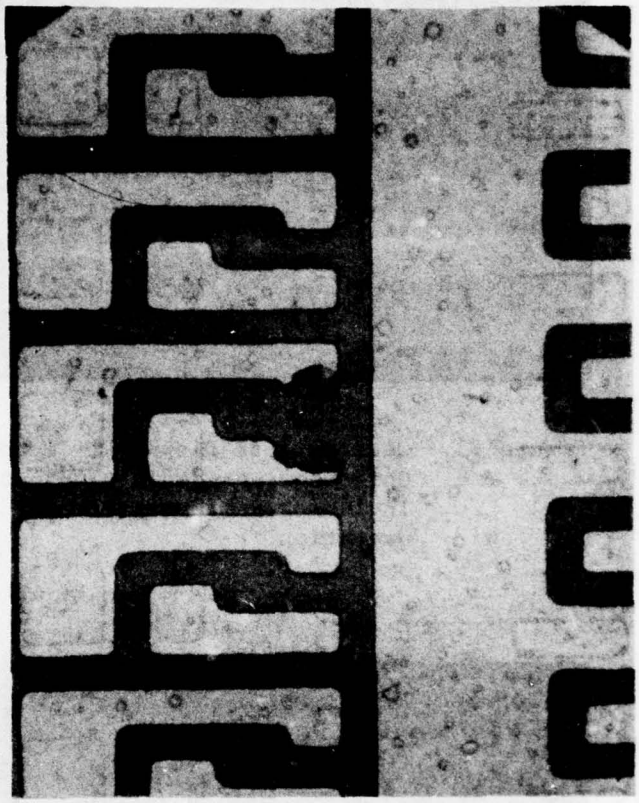


Figure 74. Aluminum Etch Defect in MMI 5086 Chip Removed from S/N 2 Hybrid Assembly.

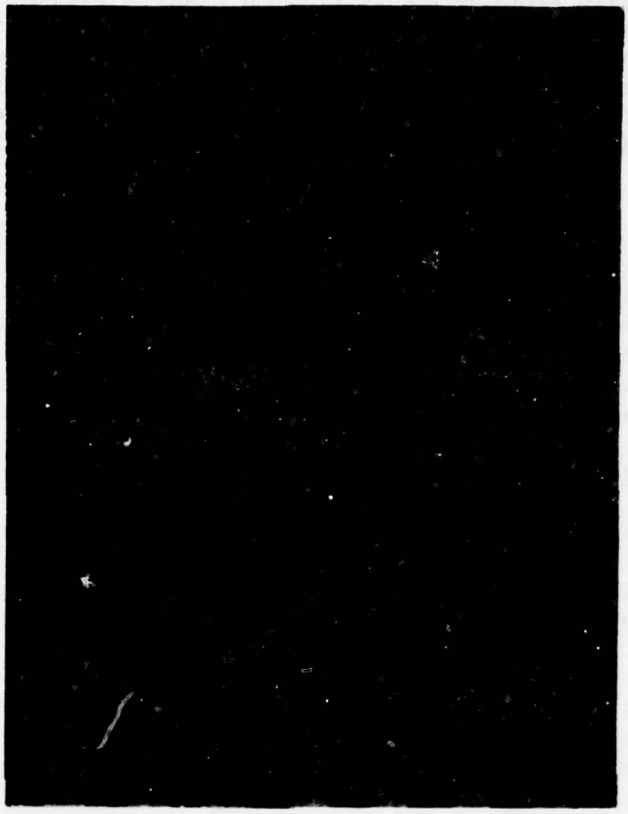


Figure 75. Amorphous Growth of Aluminum Beneath Silicon Dioxide Passivation in MMI 5086 Chip Removed from S/N 4 Hybrid Assembly.

This was the third chip bonded to the pad, indicating that the selected die bonding and outer lead bonding process provides satisfactory repairability. Further microscopic examination revealed a silicon-processing defect (see Figure 76) in the other MMI memory chip originally placed in the assembly. This second chip was replaced, and both hybrid assemblies were sealed by adding covers and then returned to test. Functional testing indicated that S/N 4 was satisfactory; so, it was subjected to the subsequent environmental testing. The second assembly, S/N 2, still had faulty outputs from one of the ROM's.

The second set of four assemblies (S/N'5 through 8) were constructed and functionally tested. All four assemblies were found to be functionally satisfactory. Covers were added to these four assemblies at GE R&DC. Subsequent functional testing indicated satisfactory operation; so, these four units were prepared for environmental and engine testing. However, one assembly, S/N 5, was found to contain an early substrate supplied prior to the use of improved pin brazing techniques. This precluded further use of S/N 5.

5. Temperature Cycling of Complete Assemblies

The temperature cycle used for this evaluation ranged from -55° to 125° C (-67° to 257° F). The cycle duration was one hour hot and one hour cold, including transit times. The oven temperature transit time from hot to cold was about 7 minutes and from cold to hot was about 20 minutes.

Initially, three assemblies (S/N'S 6, 7, and 8) were subjected to the temperature cycling. S/N 4 was added eight days later. The assemblies were tested using the hybrid module exerciser. From the start, none of the hybrid assemblies functioned at either -55° C or at 125° C. It was suspected that the MMI chips did not meet the required temperature range. In order to construct hybrids, wafers were purchased rather than dual-in-line-packages (DIP's); apparently, MMI selects the wide temperature range devices by testing the DIP's. The wafer testing at GE R&DC was done at room temperature.

Finding such a difficulty requires temperature testing at the on-tape chip or wafer level. Since no such temperature limitations had been identified and since the test would involve special, costly test equipment, the memories went directly to assembly.

Since the assemblies did not work hot or cold, continuous monitoring was stopped. Subsequently, the assemblies were checked initially at room temperature, and after each 100 cycles. S/N's 6, 7, and 8 functioned satisfactorily at room temperature after 300 cycles (600 hours). S/N 4 failed during the first 94 cycles to which it was subjected. A memory chip failure was suspected.

6. Thermal Shock Testing

Three operable and one failed unit made up the specimens available. All four of these hybrid assemblies were subjected to 50 thermal shocks. During

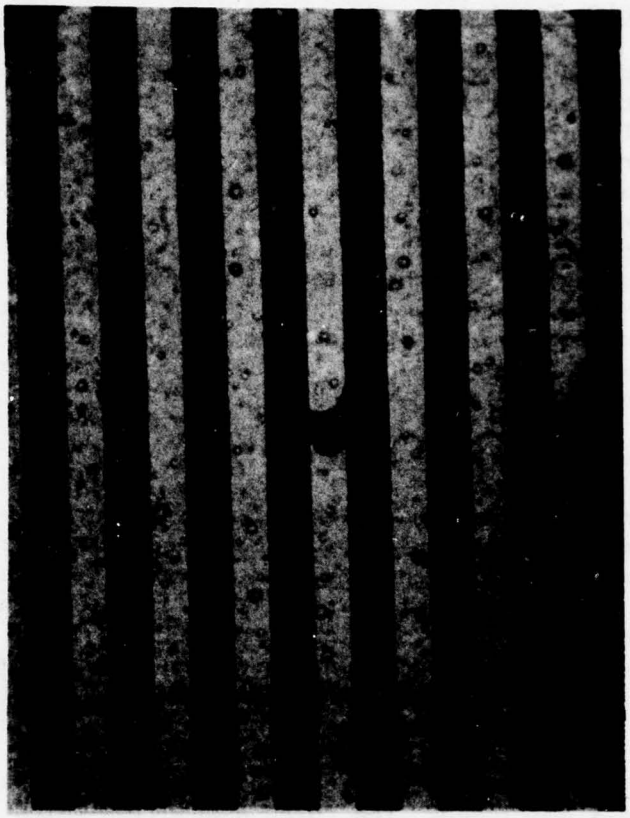


Figure 76. Aluminum Etch Defect in the Second MMI 5086 Chip Removed from S/N 2 Hybrid Assembly.

this test, the hybrid assemblies were alternately dipped in -65° and 250° F (-54° and 124° C) liquid baths. S/N's 6, 7, and 8 functioned satisfactorily at room temperature after the thermal shock test. S/N 4 remained inoperable.

7. Vibration Testing

The four hybrid assemblies, S/N's 4, 6, 7, and 8 were mounted to two aluminum brackets forming modules as discussed in Section IV.4. and as shown in Figure 65. These modules were vibrated with 0.04-inch double amplitude at 50 to 100 Hertz and at 20 g's at 100 to 200 Hertz except in the direction where transmissability was excessive. In the directions of high transmissability, the input was modified to 0.04-inch double amplitude at 50 to 100 Hertz, 20 g's at 100 to 500 Hertz, and 3 g's at 500 to 2000 Hertz. High transmissability occurred in the direction perpendicular to the mounting surfaces of the "T"-shaped aluminum bracket. The duration was three hours in each direction for a total of nine hours. Subsequent functional testing disclosed no change in performance. Additional information on the vibration test is given in Appendix A.

8. Engine Environmental Testing

The first objective of the on-engine environmental testing was to subject the hybrid assemblies to the vibration and noise characteristic of modern engines. The two modules which completed the vibration test were mounted in an F101 Central Integrated Test System (CITS) chassis. The complete assembly was mounted to an F101 engine (Serial Number 018). The CITS chassis has fuel-cooling provisions so the normal on-engine environment was provided. Figures 77 and 78 show the engine installation. The complete assembly was subjected to 30 hours and 43 minutes of on-engine endurance.

The four hybrid assemblies were then tested functionally, and no change in performance was disclosed. The three assemblies which passed the temperature cycling still functioned normally. The covers were removed from all four assemblies. The chip bonds, inner lead bonds, and outer lead bonds were inspected visually using a microscope at 140× magnification. All bonds appeared satisfactory. Figures 79 through 82 are photographs of the assemblies with their covers removed.

Memory chip failures or defects were inspected on hybrid assemblies S/N 2 and S/N 4. Further electrical testing indicated which chips were involved. Referring to Figure 4, the high (1's) outputs at D8, D32, D128, D256, and D512 all fluctuated anywhere between 0 and 5 volts when the ROM on the right was enabled on S/N 2. The output at D64 fluctuated between 0 and 2 volts when either ROM was enabled on S/N 4. This indicated that the above-mentioned ROM's were malfunctioning.

The suspect ROM chips, the right chip on S/N 2 and both chips on S/N 4, were microscopically examined using magnifications up to 500×. Two types of defects were found on the right chip of S/N 2 [see Figures 83(a) and (b)]. In Figure 83(a), two defects are shown which were interpreted as causing shorts between buried pads. In Figure 83(b), a series of spots is shown which

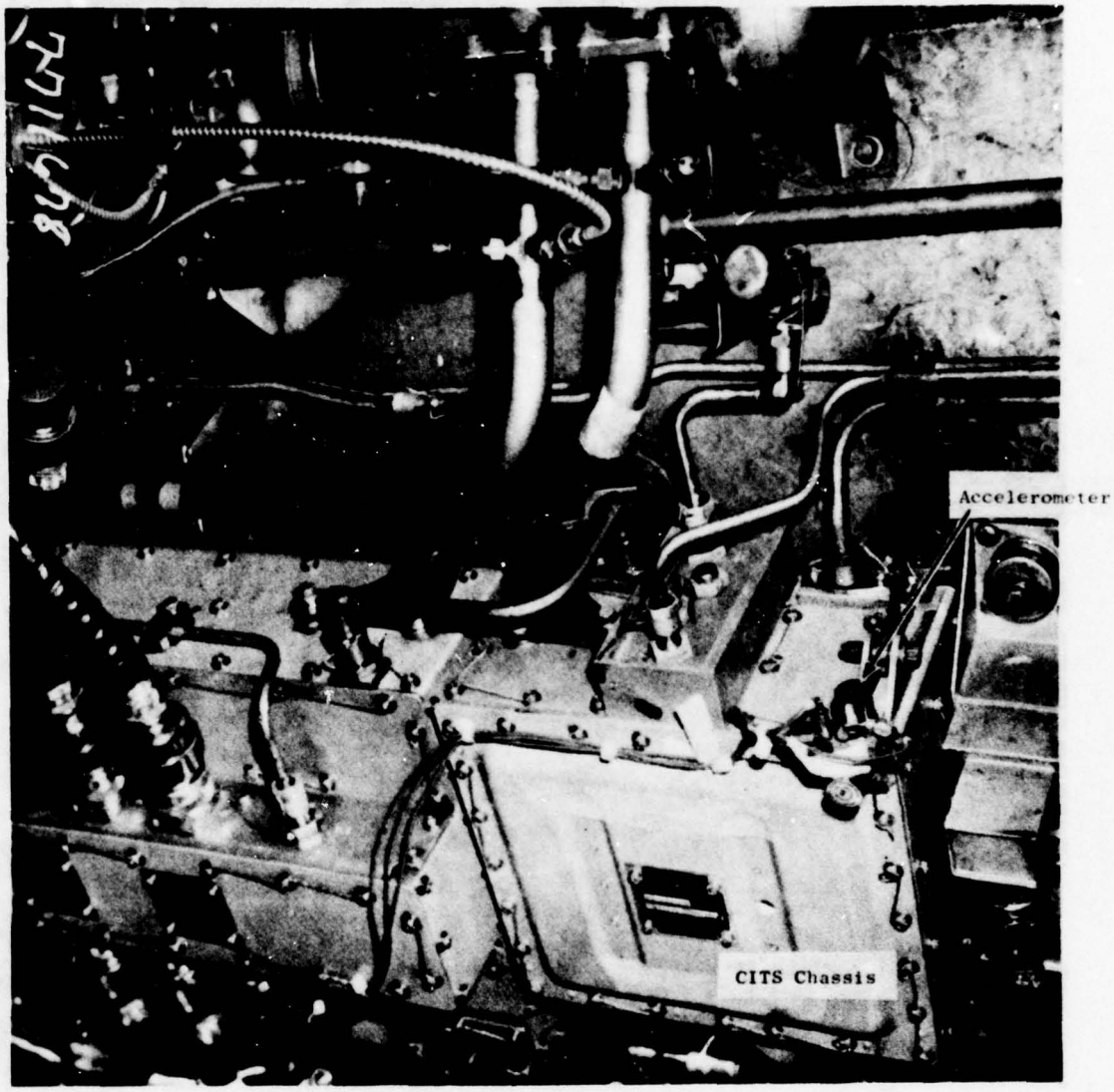


Figure 77. Closeup View Showing the CITS Chassis, Which Contained the Four Hybrid Assemblies, Mounted to an F101 Engine.

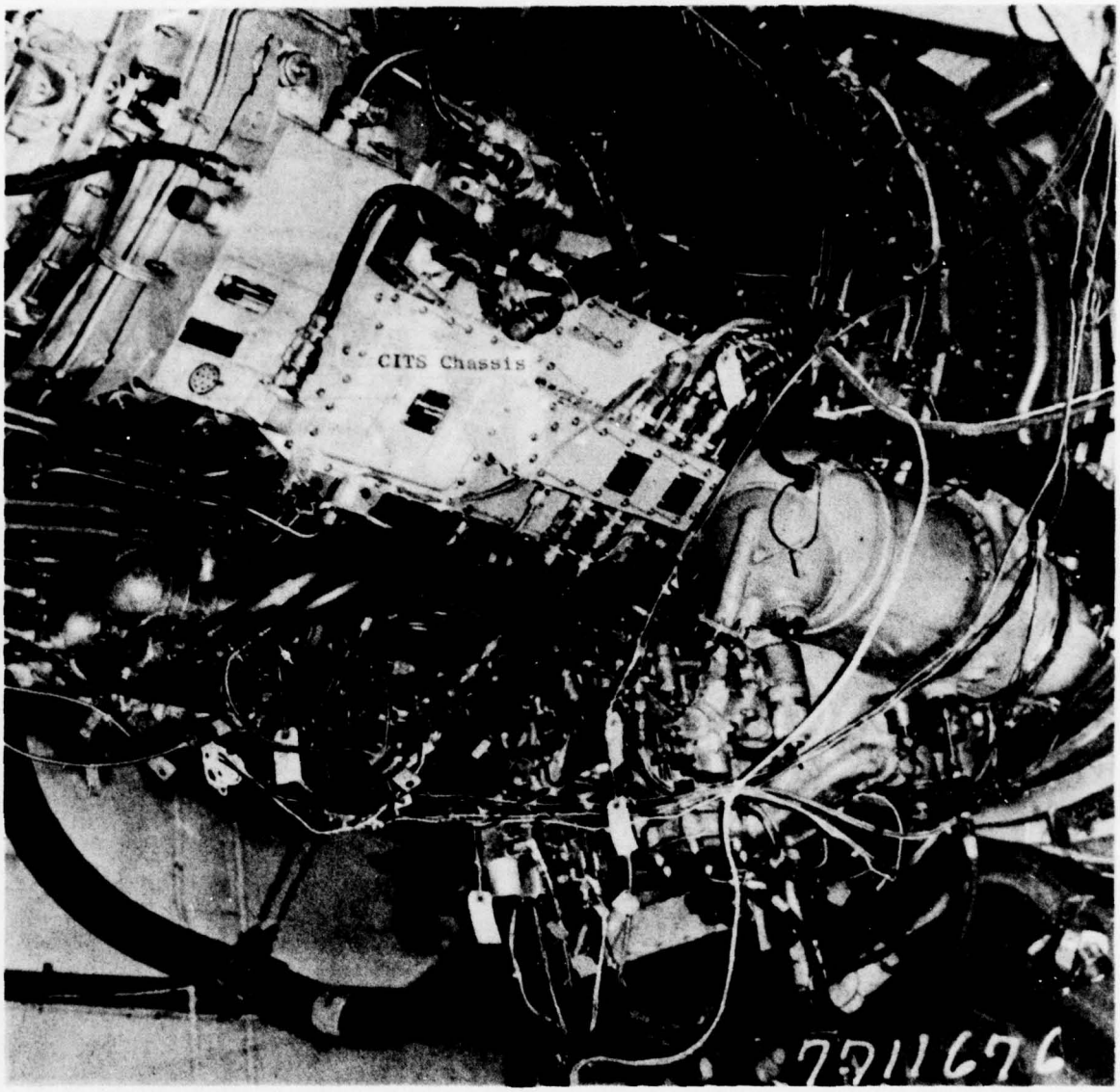


Figure 78. View of an F101 Engine Showing the CITS Chassis which Contained Four Hybrid Assemblies.

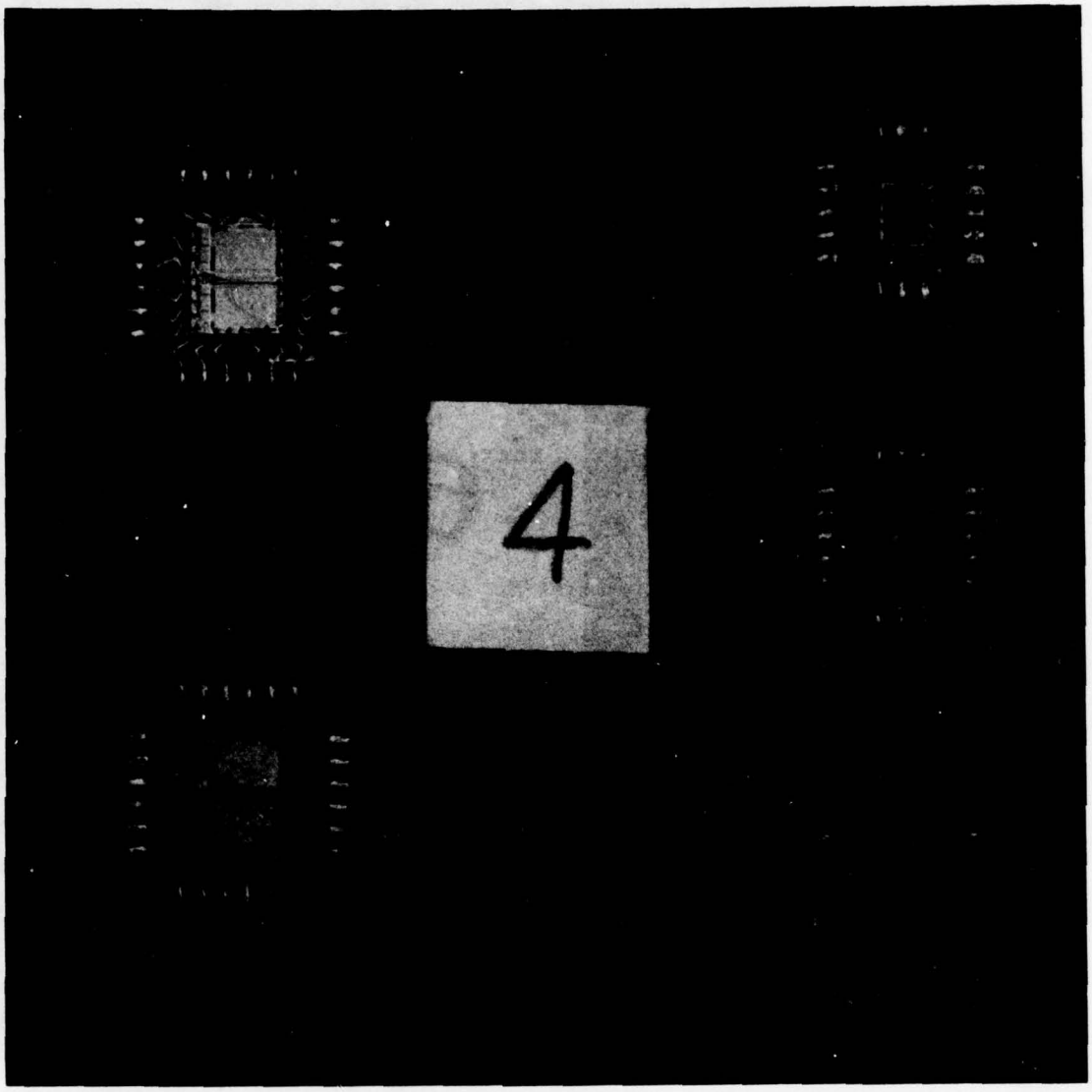


Figure 79. Photograph Showing the Active Area of S/N 4 After Testing.

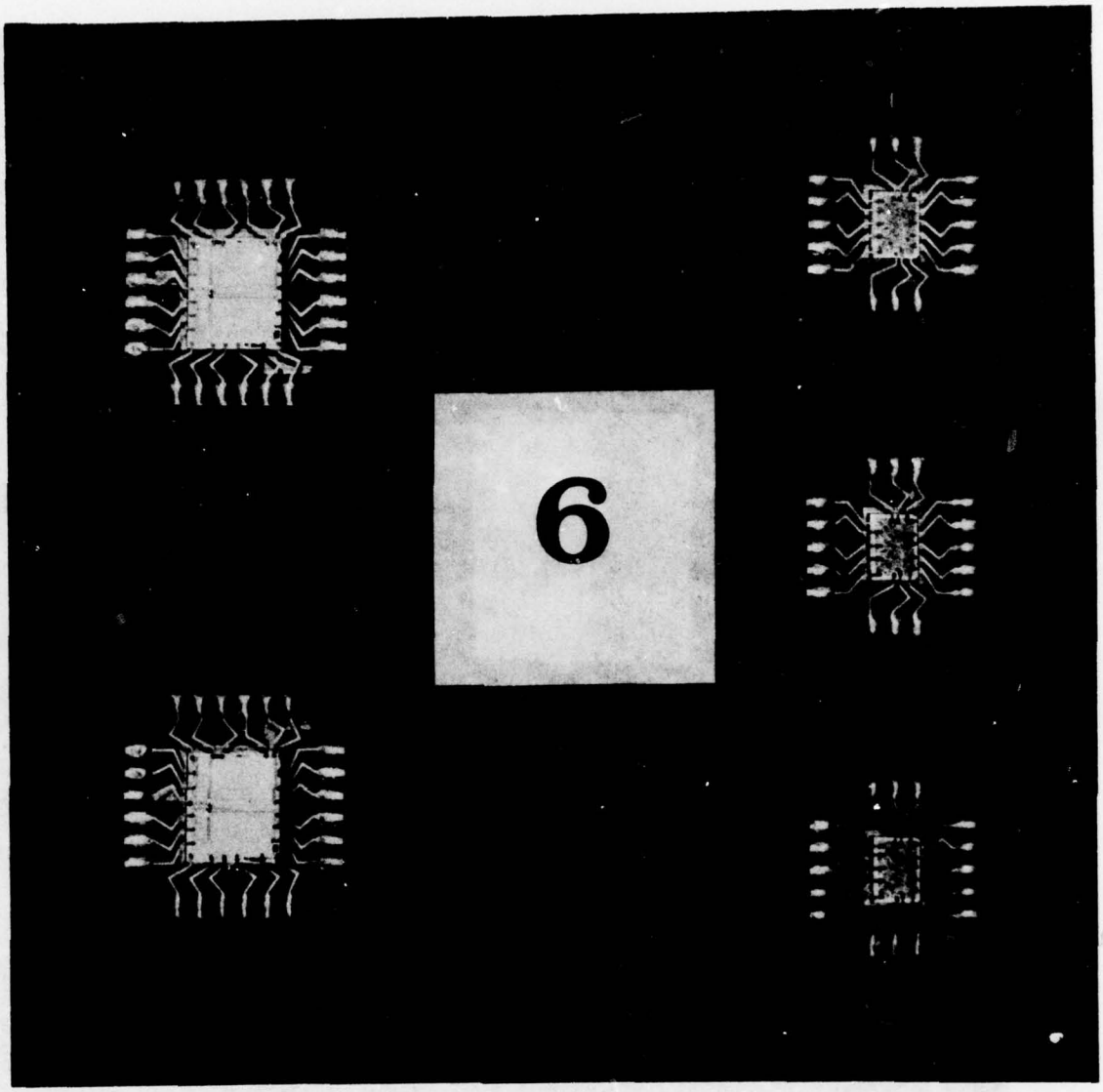


Figure 80. Photograph Showing the Active Area of S/N 6 After Testing.

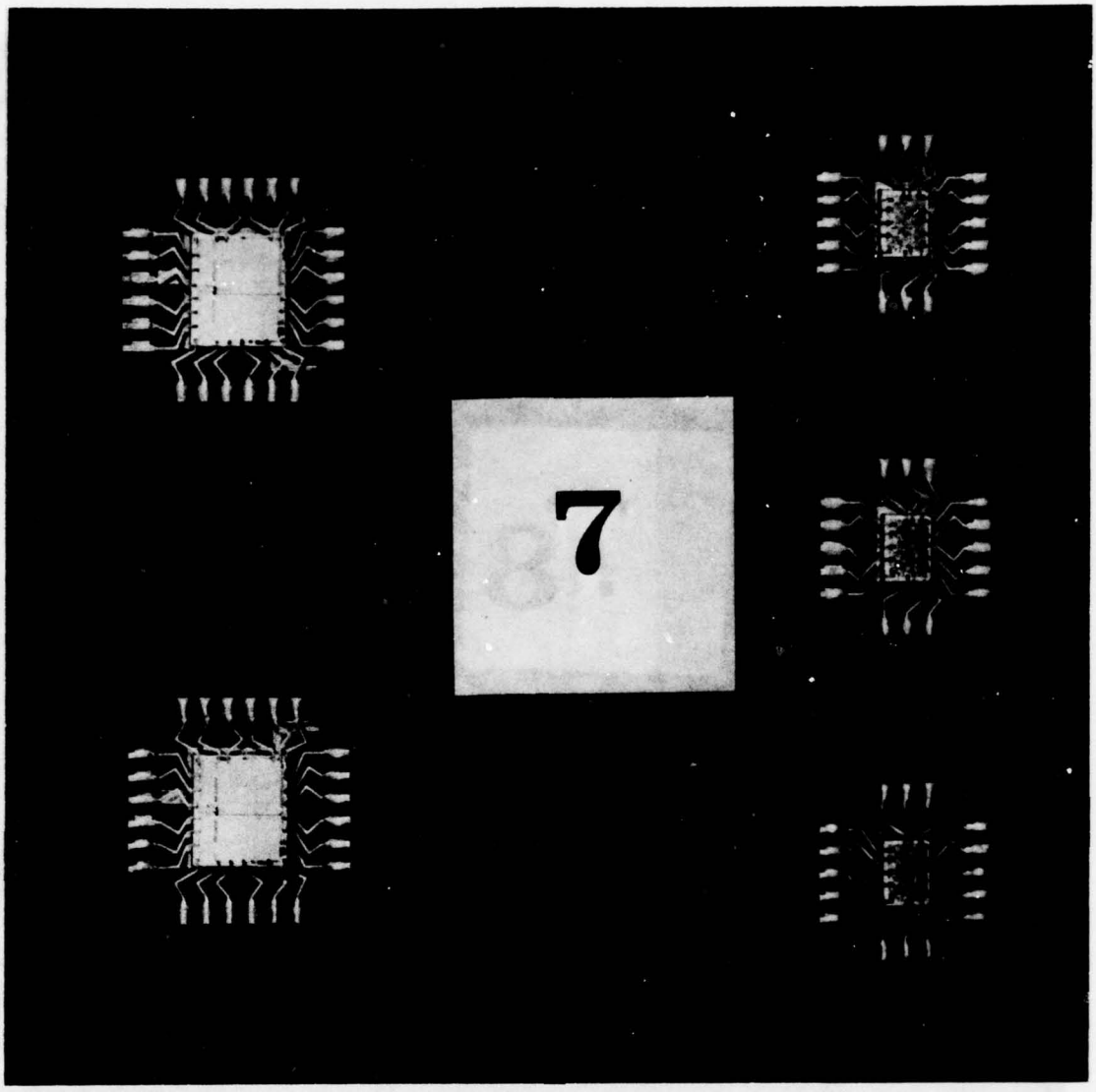


Figure 81. Photograph Showing the Active Area of S/N 7 After Testing.

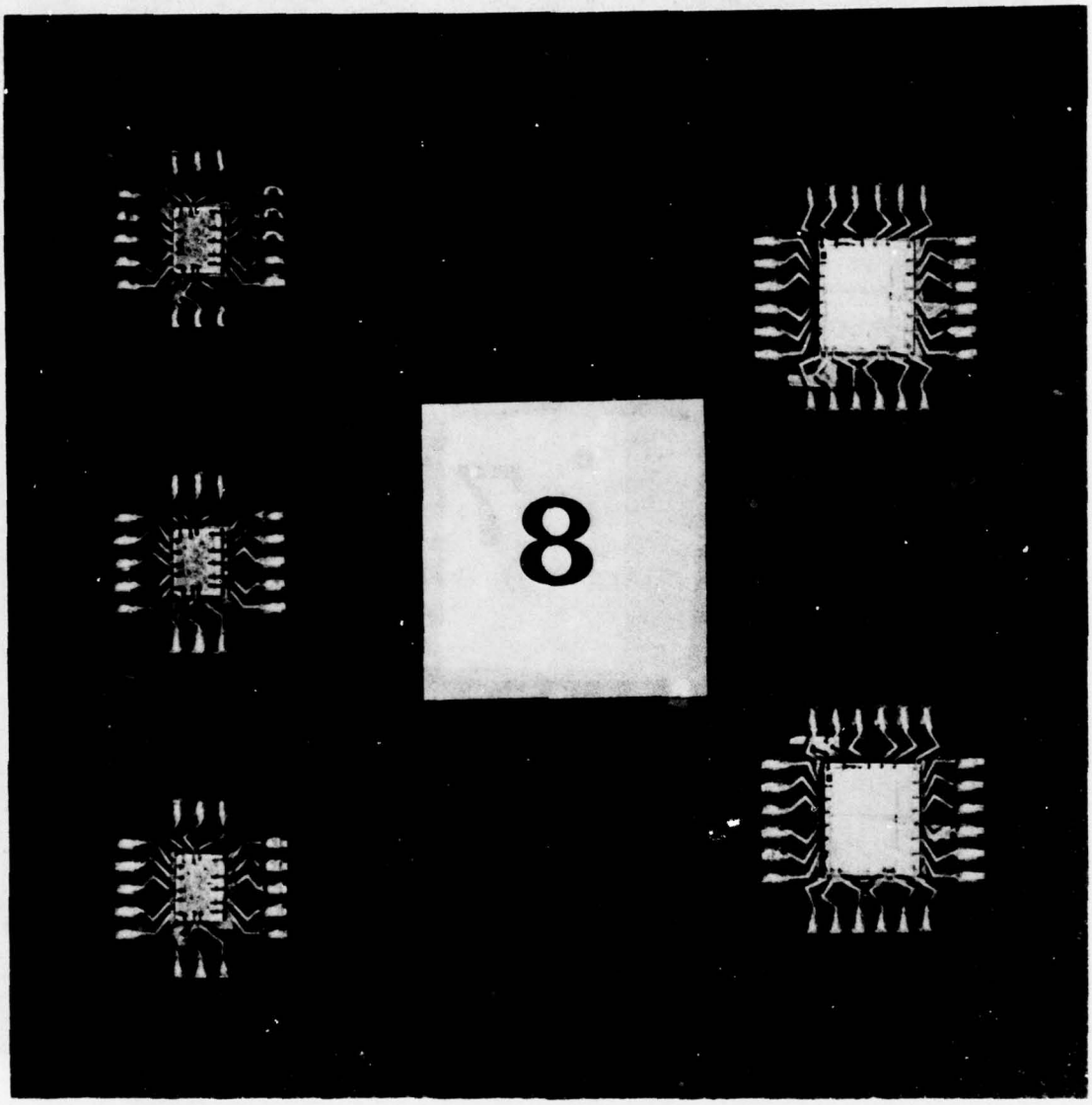
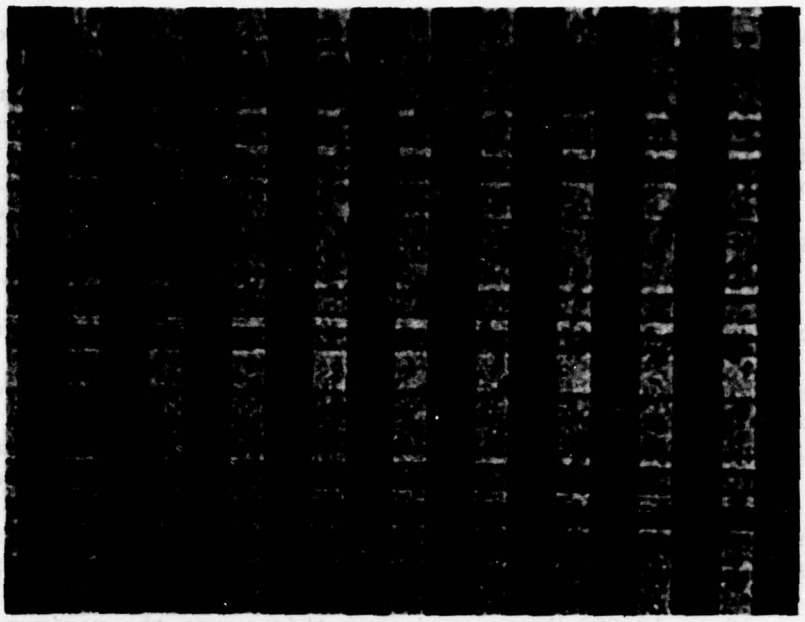
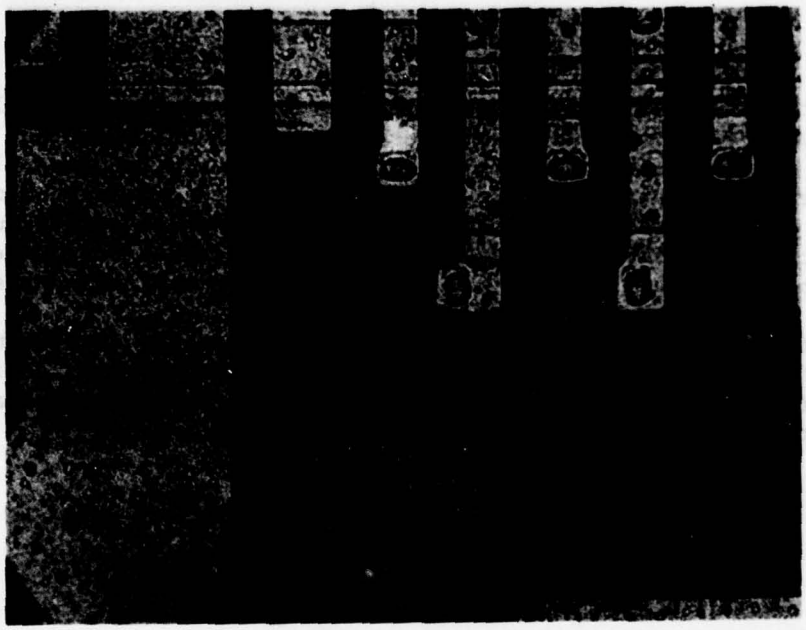


Figure 82. Photograph Showing the Active Area of S/N 8 After Testing.



(a)



(b)

Figure 83. Photograph Showing Wafer Processing Defects on the Right Chip from S/N 2.

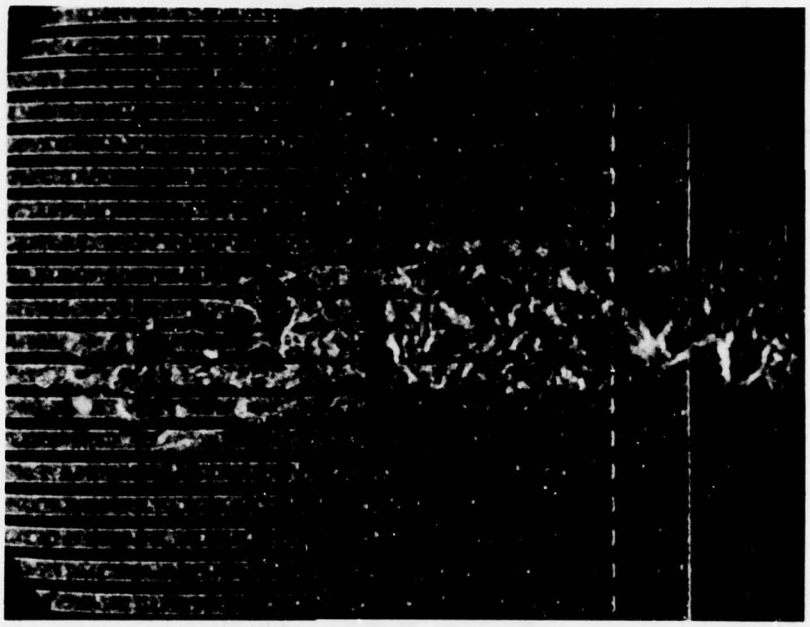
was interpreted as corrosion causing opens in the buried conductors. Figures 84(a) and (b) show the defects found in the left and right chips of S/N 4. Figure 84(a) shows several distorted conductors apparently causing shorts. Figure 84(b) shows defects which were interpreted as causing shorts between buried pads similar to those found in the right chip of S/N 2 [Figure 83(a)]. These chip defects correlate with electrical testing done to isolate the problems. This is considered sufficient evidence that the problems encountered in S/N's 2 and 4 were due to the ROM chip defects and not to the hybrid packaging approach.

A second objective of the on-engine test was the measurement of the vibration spectrum to which the hybrid assemblies were subjected and which might be expected during future on-engine applications. Three accelerometers, one for each direction, were attached to the chassis as shown in the photograph Figure 77. The accelerometers available had a frequency range capability of 10 to 10,000 Hertz. The triaxial vibration was recorded on tape. Data were obtained at four fan speeds from 40% to 100% rated (7570 rpm). The predominant fan duct vibratory excitation corresponded to the first stage fan blade passing frequency of 50 per revolution and a second stage fan blade passing frequency of 88 per revolution. The range of excitation frequencies recorded was 10 to 10,000 Hertz, and over this range the maximum recorded value was 10 g's at 4400 Hertz. More detailed information is given in Appendix B.

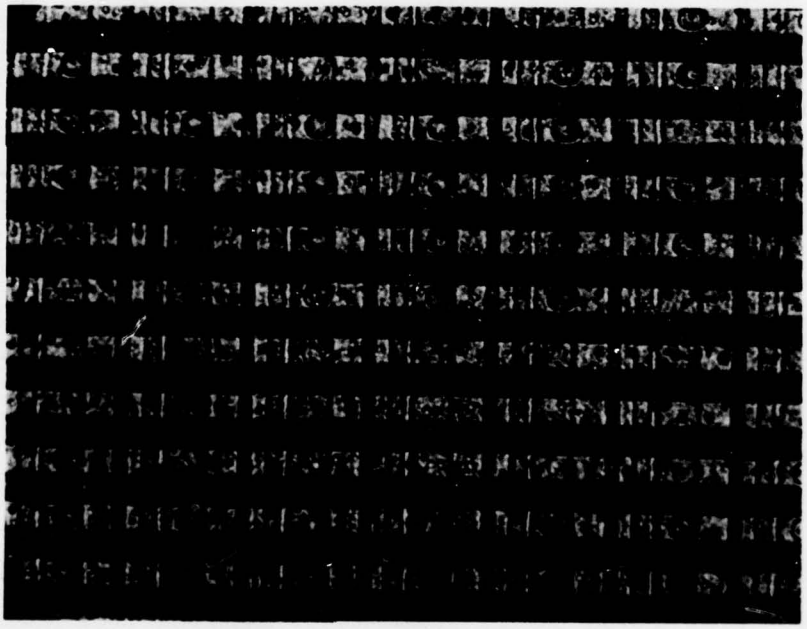
9. Summary of Test Results

A total of eight hybrid assemblies was made. The test results are summarized by Table 10. Three assemblies contained substrates that were not processed using the improved pin brazing techniques. Two assemblies, even though they were repaired before sealing, contained defective memory chips; one which did not pass functional testing and one which failed during temperature cycling. The three assemblies which contained substrates using the improved pin brazing technique and satisfactory memory chips passed all tests.

The same three assemblies were examined microscopically at 140× magnification, and all the chips, inner-lead, and outer-lead bonds appeared satisfactory. The test results verify that the selected hybrid packaging approach is well suited for digital electronic engine controls.



(a)



(b)

Figure 84. Photographs Showing Wafer Processing Defects on Both Chips from S/N 4.

Table 10. Summary of Test Results.

Assembly	Functional Test, Uncovered	Repair	Functional Test, Covered	Thermal Cycling	Thermal Shock	Vibration Test	Engine Test
S/N 1	Pin Joints Failed	---	---	---	---	---	---
S/N 2	(1) Failed	(1) Chip Replaced	Failed (3)	---	---	---	---
S/N 3	Pin Joints Failed	---	---	---	---	---	---
S/N 4	Failed	(2) Chip Replaced	Passed	(3) Failed (<90~)	---	---	---
S/N 5	Passed	None	Passed	Pin Joints Failed Brazing	---	---	---
S/N 6	Passed →						
S/N 7	Passed →						
S/N 8	Passed →						

(1) ROM chip replaced twice, once for etch defects and once for handling damage.

(2) ROM chip had growth-shorting conductors.

(3) ROM chip failure verified.

SECTION VI

CONCLUSIONS

The objective of the Hybrid Packaging of Integrated Circuits Program was to design and to develop a hybrid packaging approach especially suited for on-engine digital electronic engine controls. Based on the results of the design studies, material investigations, process developments, fabrication, and testing, the following conclusions can be reached:

1. Gold-tin fusion-type inner lead bonds were made readily on chips from wafers that were bumped by the General Electric Company and Fairchild Camera and Instrument Company. The bonds were made using an inner lead bonder and they performed successfully in test.

2. Lead-indium reflow chip bonds and outer lead bonds were made readily using a hot plate. These bonds also performed successfully in test.

3. Pin bond tests made on substrates fabricated by the processes developed in this program indicated that high strength pin/substrate joints can be made using 0.045 inch square pins.

4. This program encountered chip processing and temperature difficulties and these difficulties encumbered the environmental testing. Nevertheless, the resulting hybrid assemblies did provide a successful demonstration of integrated circuit packaging.

5. This program took a "first look" at a hybrid microelectronic package constructed by TAB techniques wherein matched thermal coefficients were obtained through Kovar leads. This advanced the technology in a direction which could be useful to future aircraft engine controls. Like all hybrid developments, this is a first step, the complete development of such a package and its associated fabrication processes will involve a considerable number of step by step engineering projects.

APPENDIX A

ENVIRONMENTAL EXPOSURE

CERTIFICATION

Report No. 17[illegible]

CINCINNATI ELECTRONICS
2630 GLENDALE-MILFORD ROAD, CINCINNATI, OHIO 45241 U.S.A. TEL (513) 563-6000 TWX 810 464-8151

Date: 23 MAY 1977

ENVIRONMENTAL EXPOSURE CERTIFICATION

CUSTOMER GENERAL ELECTRIC COMPANY C. E. Corp. Product: 960513

Customer P.O. No. 17K43597

Specimen(s) HYBRID ELECTRONIC ASSEMBLIES

Part No. HCD-1126

Serial No. NONE

Test specimen(s) were subjected to the environments noted below:
Vibration: 50-100 Hz, 0.04 in.double amplitude, 100-2000 Hz 20g's, except in axes where transmissability was excessive per General Electric personnel evaluation. Modified vibration schedule 50-100 Hz 0.04 in.double amplitude, 100-500 Hz 20 g's, 500-2000 Hz 3 g's. Three hours vibration per axis for a total of nine hours.

Data is recorded in Engineering Notebook 4334 Pages 59

Remarks: There was no visual evidence of damage after vibration.

Test Conducted By: R. Marasco
R. Marasco

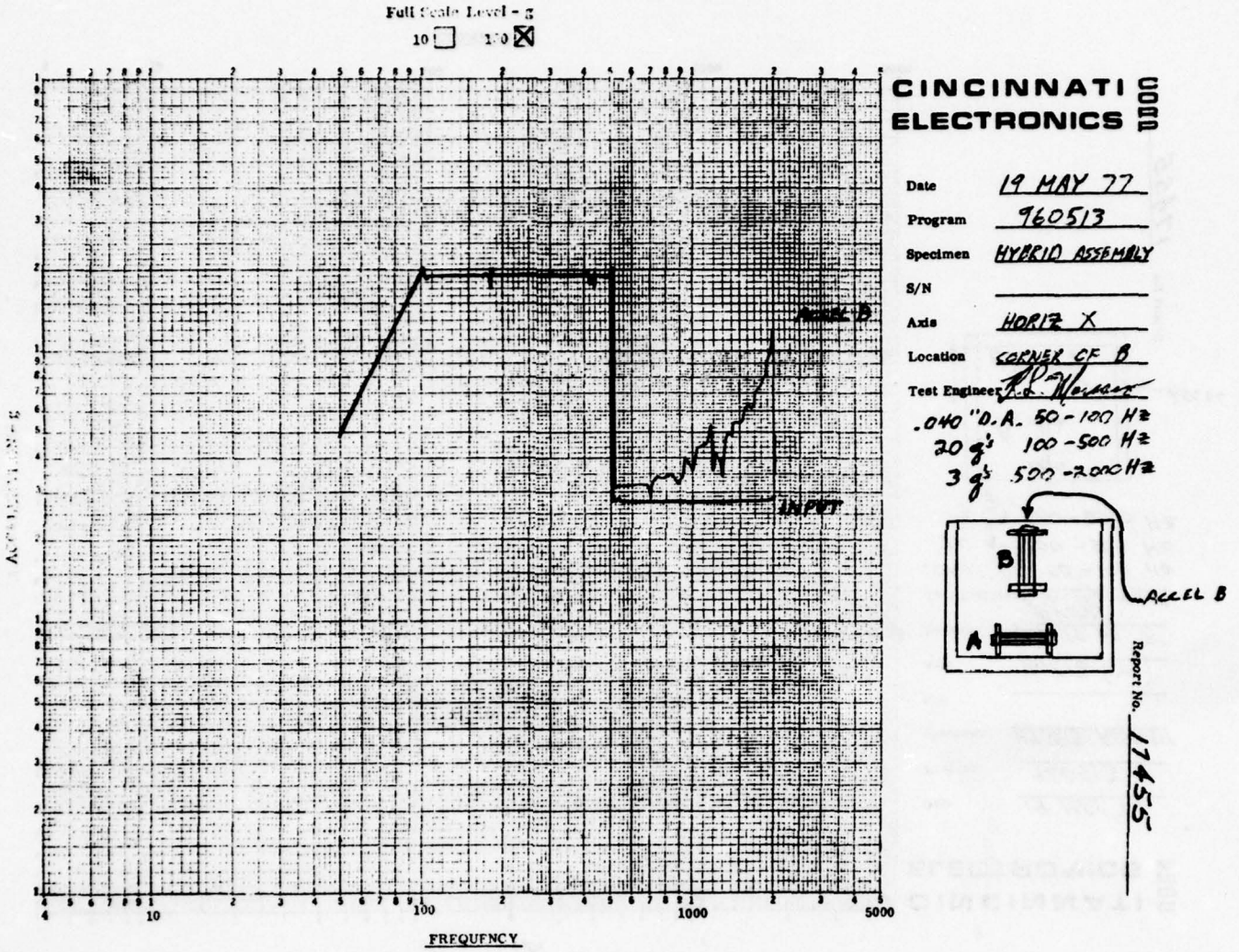


Figure A-1. Response at Corner of Module B to X Input.

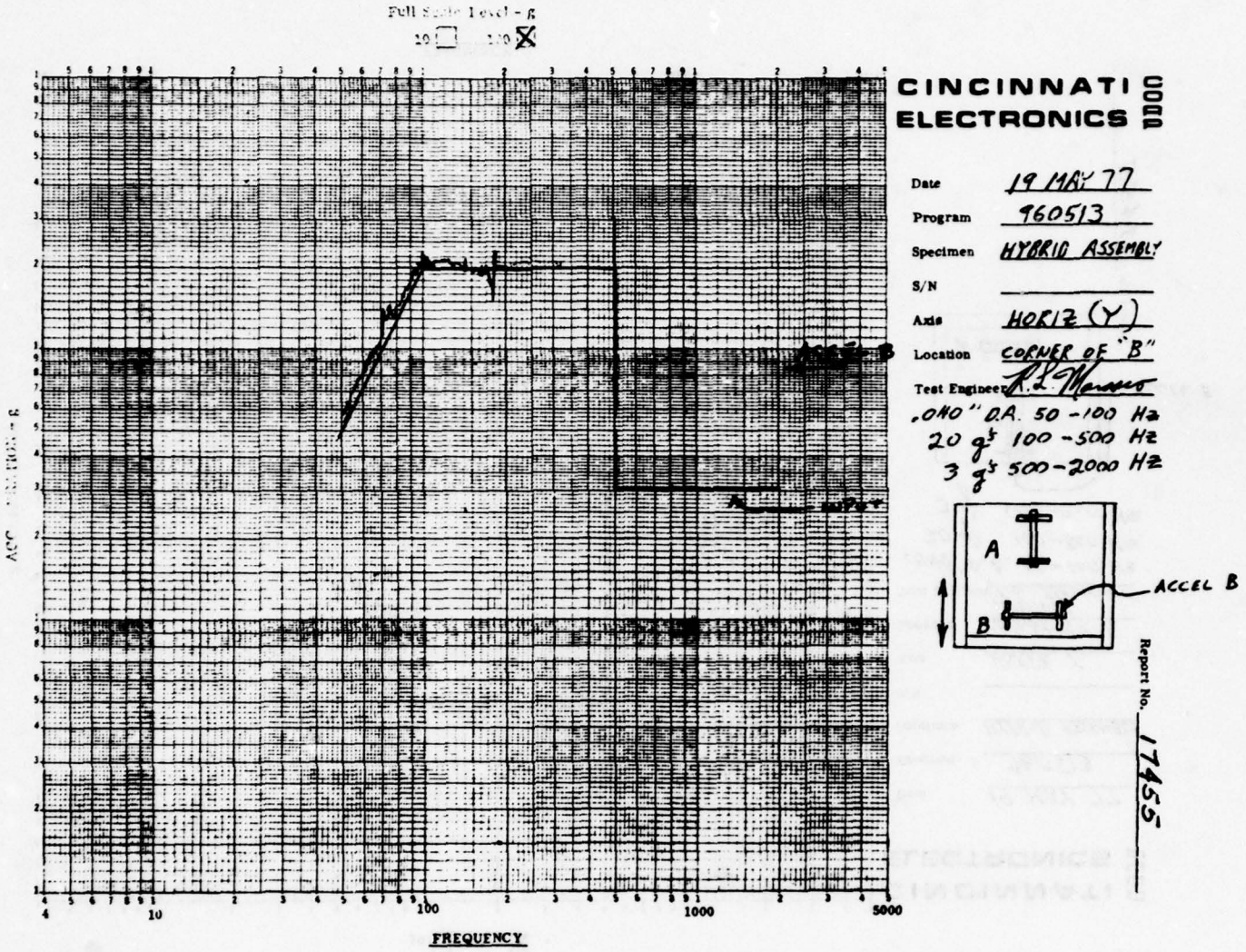


Figure A-2. Response at Corner of Module B to Y Input.

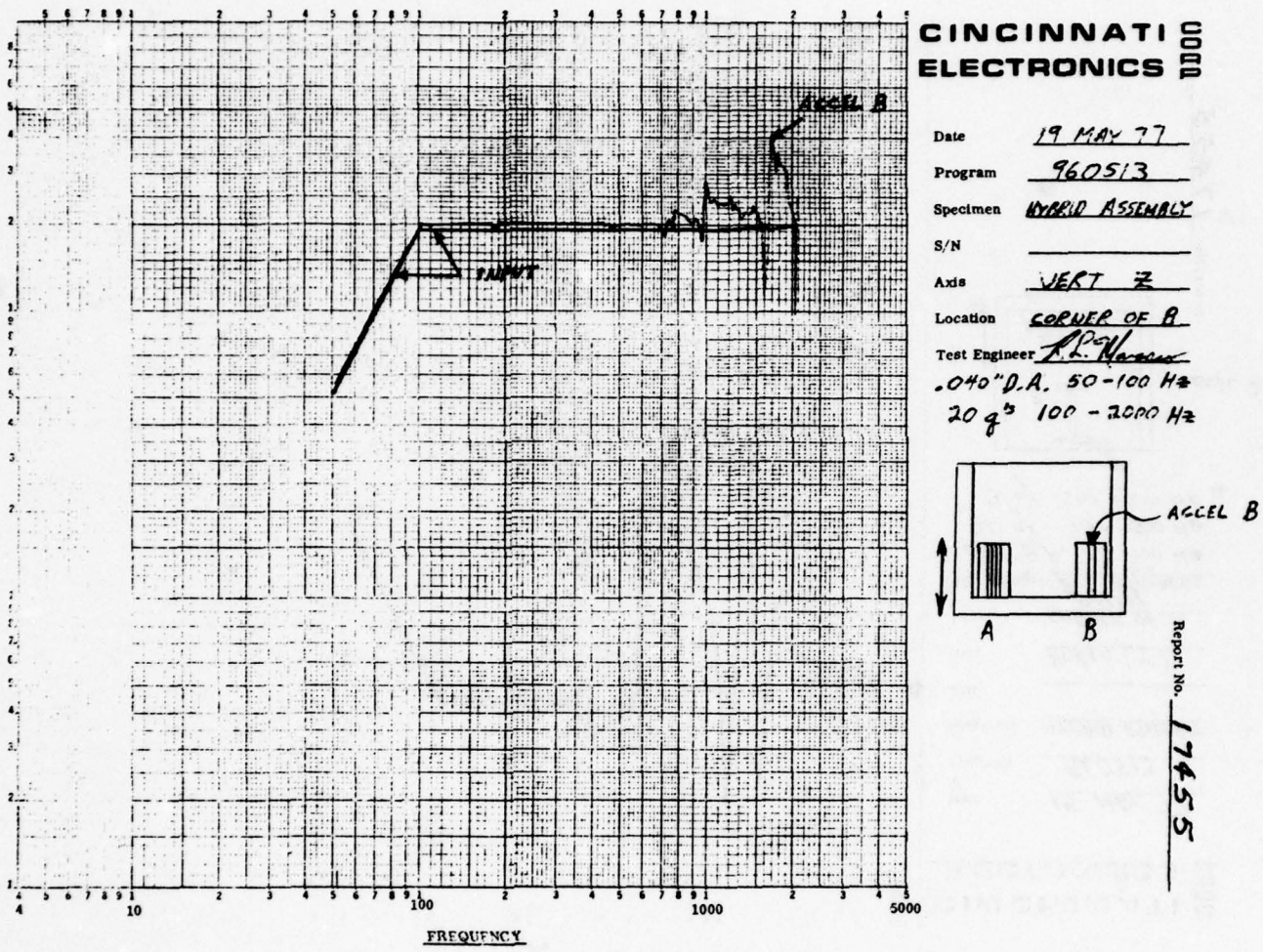


Figure A-3. Response at Corner of Module B to Z Input.

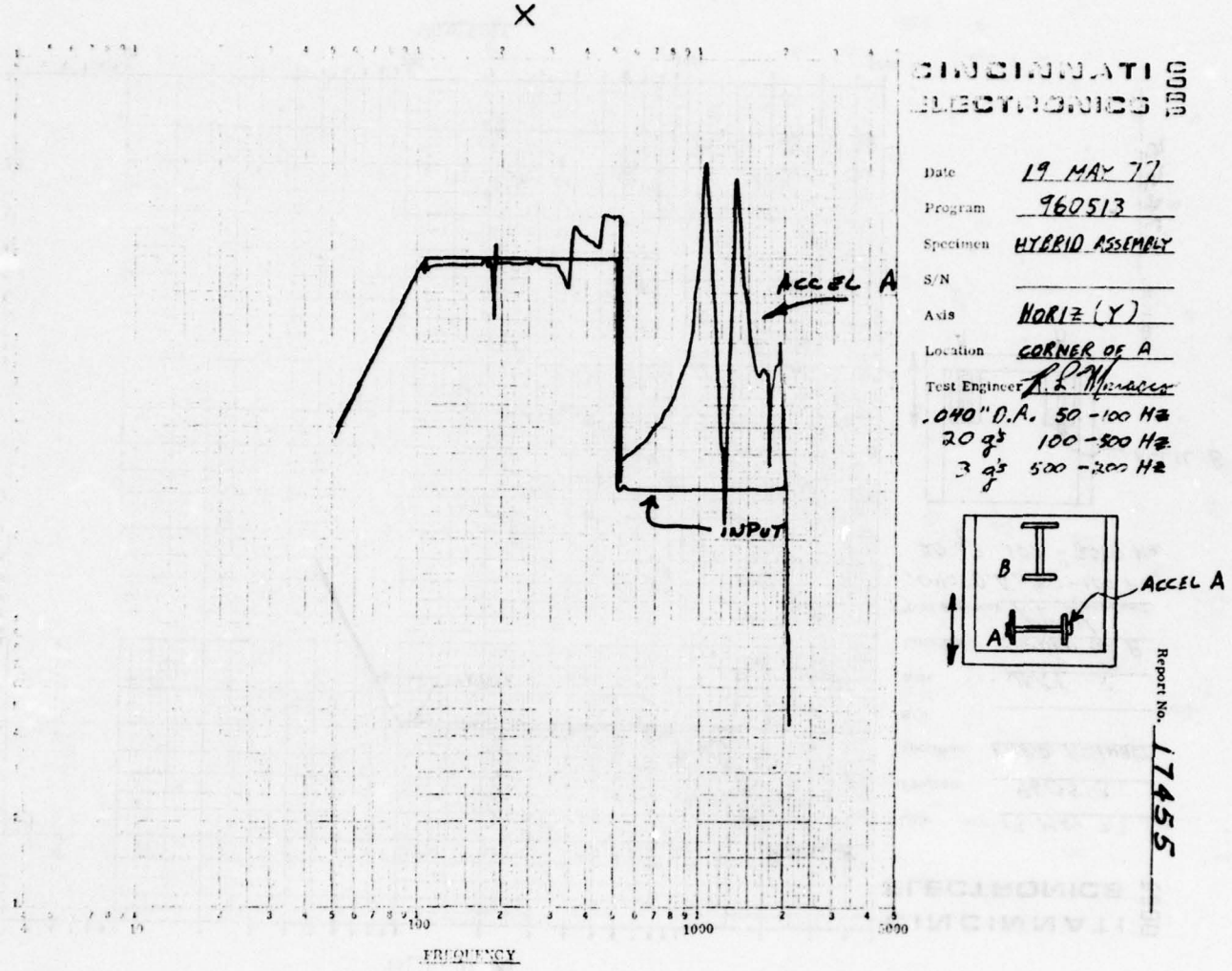


Figure A-4. Response at Corner of Module A to Y Input.

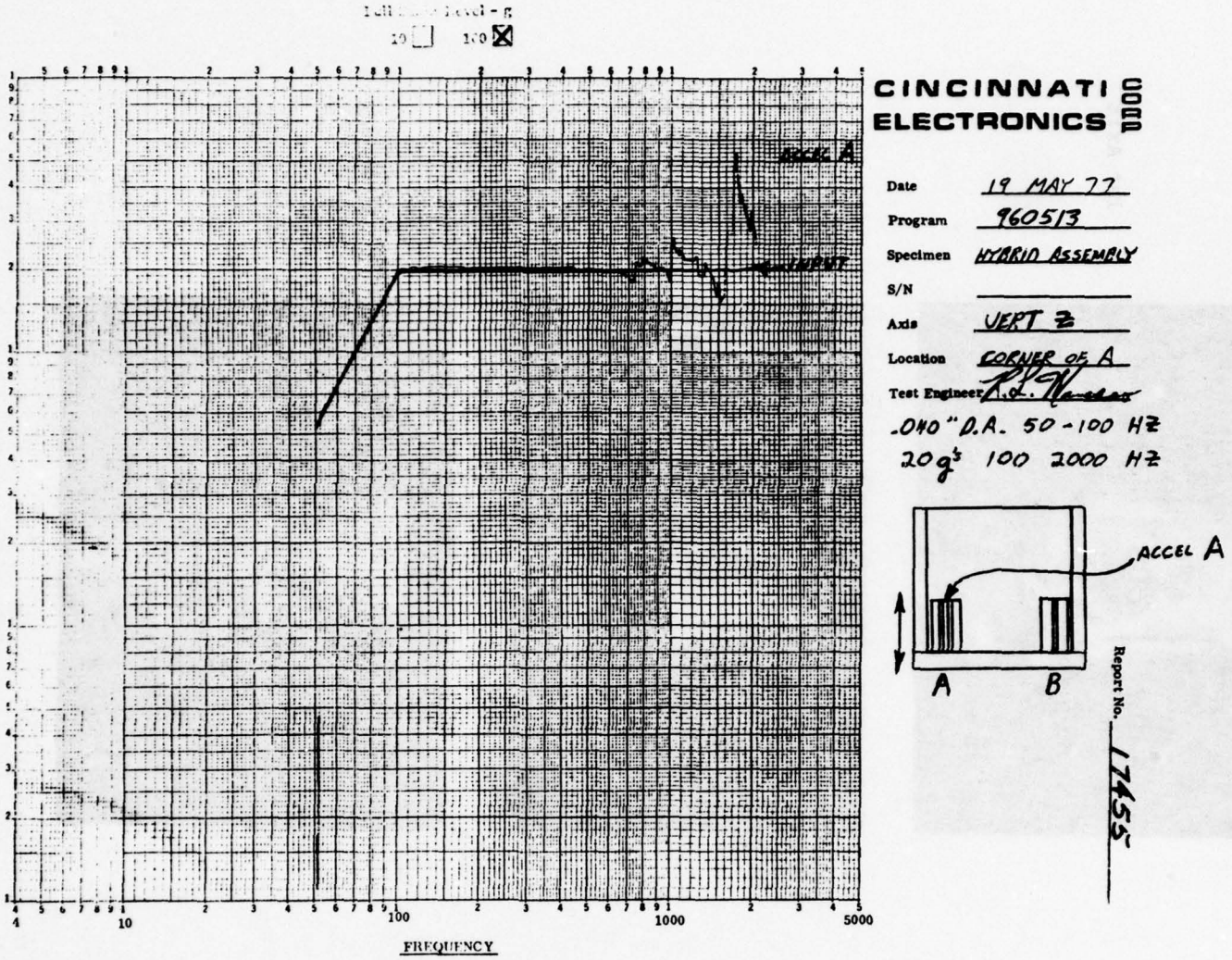
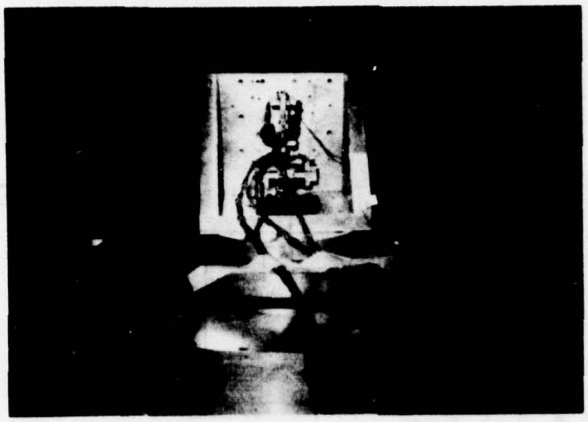
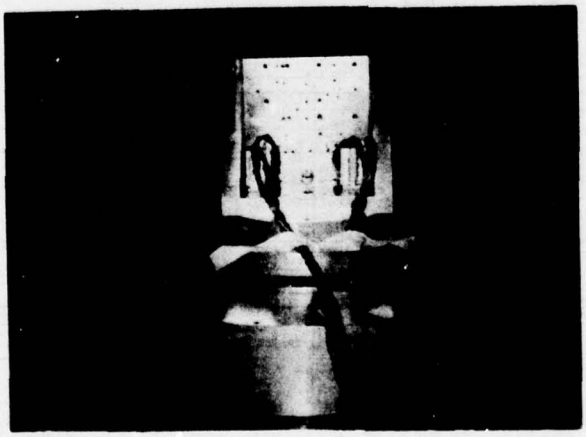


Figure A-5. Response at Corner of Module A to Z Input.



1st Axis

2nd Axis



3rd Axis

Figure A-6. Photographs Showing the Three Axes.

APPENDIX B - ON-ENGINE VIBRATION TEST DATA

1. Introduction

In the future, increasing use will be made of electronic controls which are mounted onto aircraft gas turbine engines. A major control packaging design goal has been and must continue to be to avoid electronic component failure as the result of engine induced mechanical vibrations. The mode of failure may involve motion of the component, such as a resistor or capacitor, which in turn stresses and fatigues the solder joint. In the case of microelectronics, the problem may involve resonant vibration of the chip-to-substrate lead and a subsequent "open" failure. Vibration could also induce cracks in hermetic seals of electronic components which may lead to failure by means of corrosion.

To prevent vibration problems, it has been customary to pot the electronic components including wire connections in an elastomer compound such as silicone rubber. The potting compound provides some degree of isolation dampening although mechanical connection usually exists to the base of the control chassis. The potting compound also provides vibration energy dissipation and helps to restrain the electronic component. Potting is a proven technique for avoiding vibration problems. This is shown by the F101 engine electronic control experience. For this program none of the failures to date are attributed to vibration.

Vibration isolation dampeners may be considered as an alternative to potting compound. Dampeners may be located at the chassis mounts and also within the control. Dampeners are intended to eliminate transmission of vibrations over the frequency range which could cause resonance of a structure, component, or subassembly inside the control. Acoustic noise can still be transmitted to the components, however.

In order to realistically design and test engine mounted electronic components and controls, it is necessary to determine the magnitude and frequencies of engine vibrations. This report contains vibration data for the F101 engine titanium stress skin fan duct. The results indicate that strong resonance-producing vibration excitation may be expected at frequencies up to 10,000 Hz. Maximum G-levels are tabulated below. These results indicate a definite need for potting or dampening as a means for avoiding vibration damage to engine-mounted electronic components. The results of this report are not intended to establish design requirements or maximum vibration level requirements. Design reqquirements must also consider engine unbalance, bird strike unbalance, and possibly higher vibration locations on the engine.

2. Test Setup

The F101 engine includes an engine central integrated test system (CITS). The electrical signal processor unit used for this system is mounted to the engine fan duct. As part of an Air Force sponsored program to evaluate hybrid electronics, alumina substance boards with electrically interconnected hybrid chips were placed inside a CITS chassis and subjected to engine vibrations.

Figures B-1 through B-3 show the CITS chassis P/N 4013145-274G01 mounted to the fan duct of F101 engine 470018, Build 3. The CITS chassis is situated approximately six feet aft of the two-stage engine fan. The chassis is rigidly attached to the titanium stress-skin duct used on this engine. The duct wall construction consisted of two 0.015-inch titanium sheets brazed to either side of 0.0035-inch thick honeycomb sheet. Overall wall thickness is 0.400 inch. The four mounting points for the CIT chassis consisted of 1.25-inch-diamter welded-in bosses.

3. Test Runs

F101 engine 470018 made a series of steady-state runs at speeds from idle to max dry during the months of December 1977 and January 1978. CITS vibration data were recorded during these runs. These data consisted of magnetic tape recordings of overall G-level in the engine axial, radial, and tangential directions.

4. Interpretation of Data

Vibration data was obtained from piezoelectric accelerometers mounted to the test component. These accelerometers are accurate to ±5 percent of output value at G-levels from 1 to 6000 Hz. From 6000 to 10,000 Hz, accelerometer accuracy is within +10 percent of output value. Considering all error sources, the accuracy of plotted data is ±10 percent below 6 kHz and +15, -5 percent above 6 kHz. Accelerometers for frequencies higher than 10 kHz were not available at GE Evendale when this test was requested.

The overall level of acceleration was recorded on magnetic tape at various steady-state engine speeds. This overall G-level corresponds to the actual vibration motion of the test part as seen by the accelerometer. This motion is the result of numerous periodic vibrations each of which may be assumed to be individual sinusoids of a particular frequency. Figure B-4 shows a typical trace of magnetically recorded overall G-level. It is customary to express the overall value in terms of peak G's which corresponds to the highest value of acceleration recorded during the time period. The width of the curve corresponds to the difference between this maximum (peak) and minimum G's. The value of overall G's is not meaningful in terms of resonant frequency vibration and should not be used to calculate displacement or velocity since this real complex vibration is not sinusoidal. The phase relationship of the individual periodic vibration sources is not evident from this data. Peak G's may be attributed to phase reinforcement of different frequencies as well as from higher magnitudes of particular forcing frequencies.

In order to assess the possibility of resonant forcing frequencies and to approximate displacement and velocity in terms of discrete sinusoidal frequencies, the record of overall G-level can be spectrum analyzed. Typical results of the spectrum analysis are shown in Figure B-5. These results are obtained by scanning the magnetic tape record of overall G-level to determine the average value of peak G-levels at frequencies between 1 and 10,000 Hz. The bandwidth at each frequency is determined by dividing the spectrum (10,000 Hz) by the number of filters, in this case 500. The result is a frequency

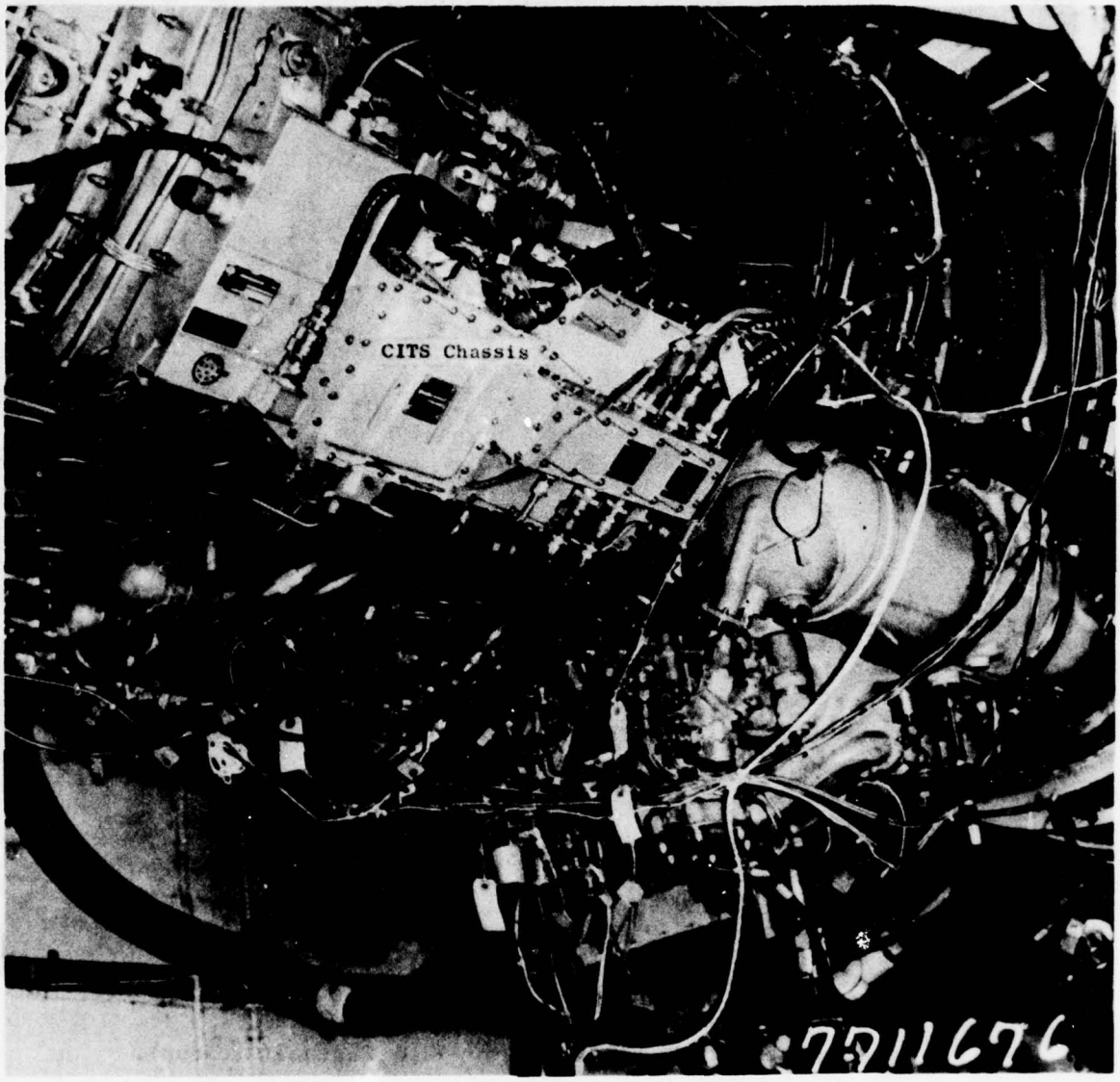


Figure B-1. CITS Mounted on an F101 Engine.

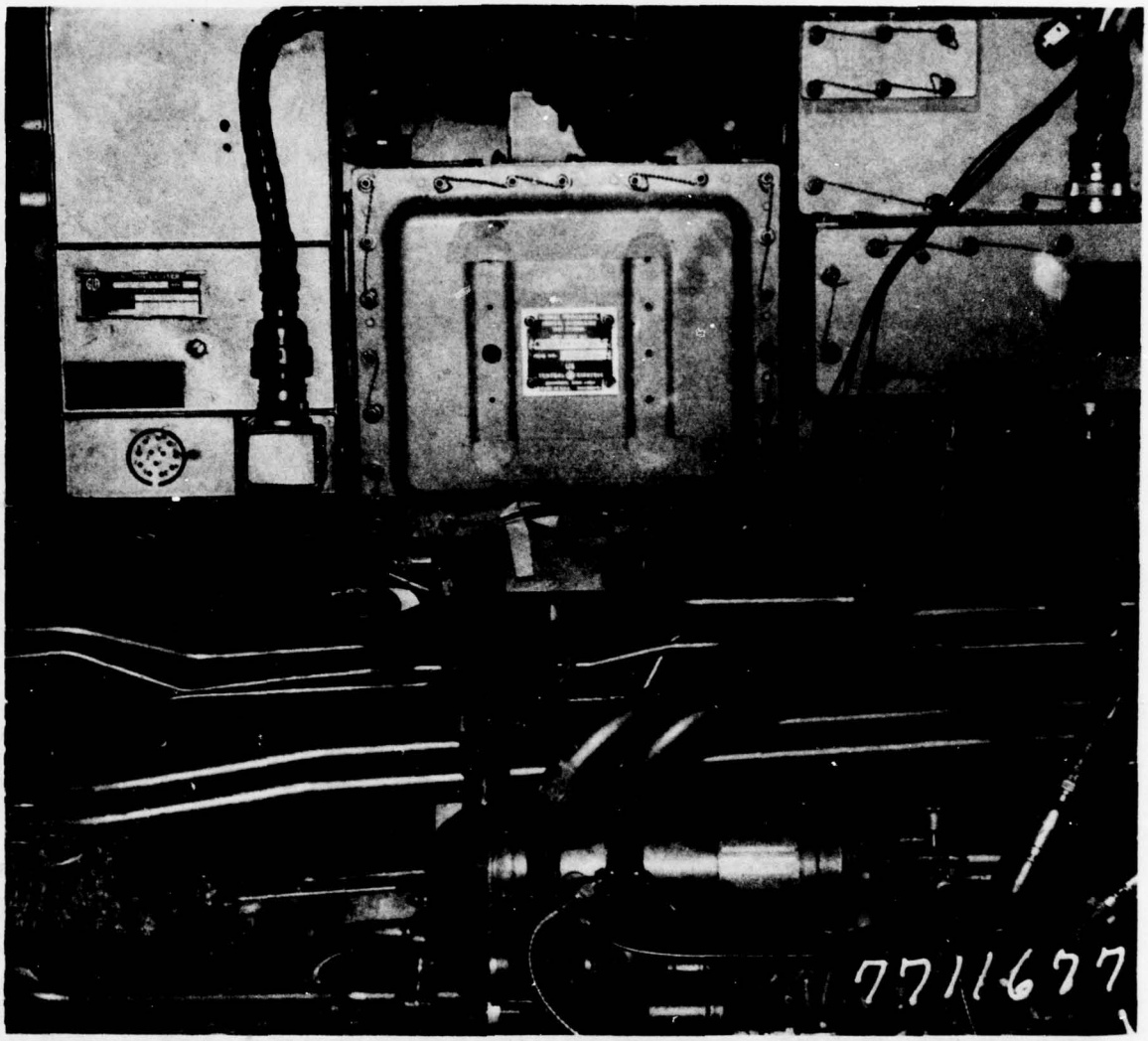


Figure B-2. CITS Mounted on an F101 Engine (Closeup).

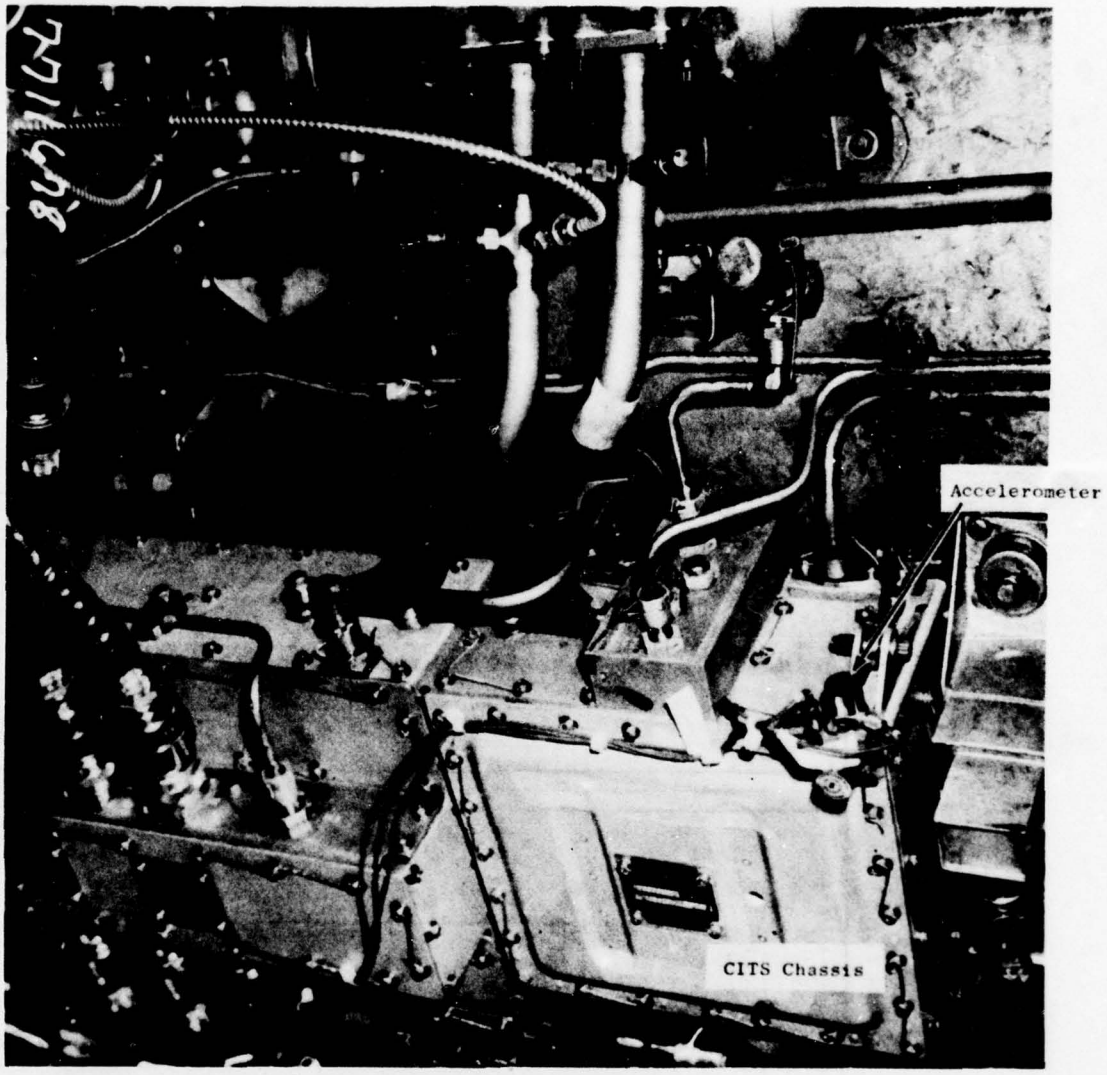


Figure B-3. Accelerometer Locations on CITS.

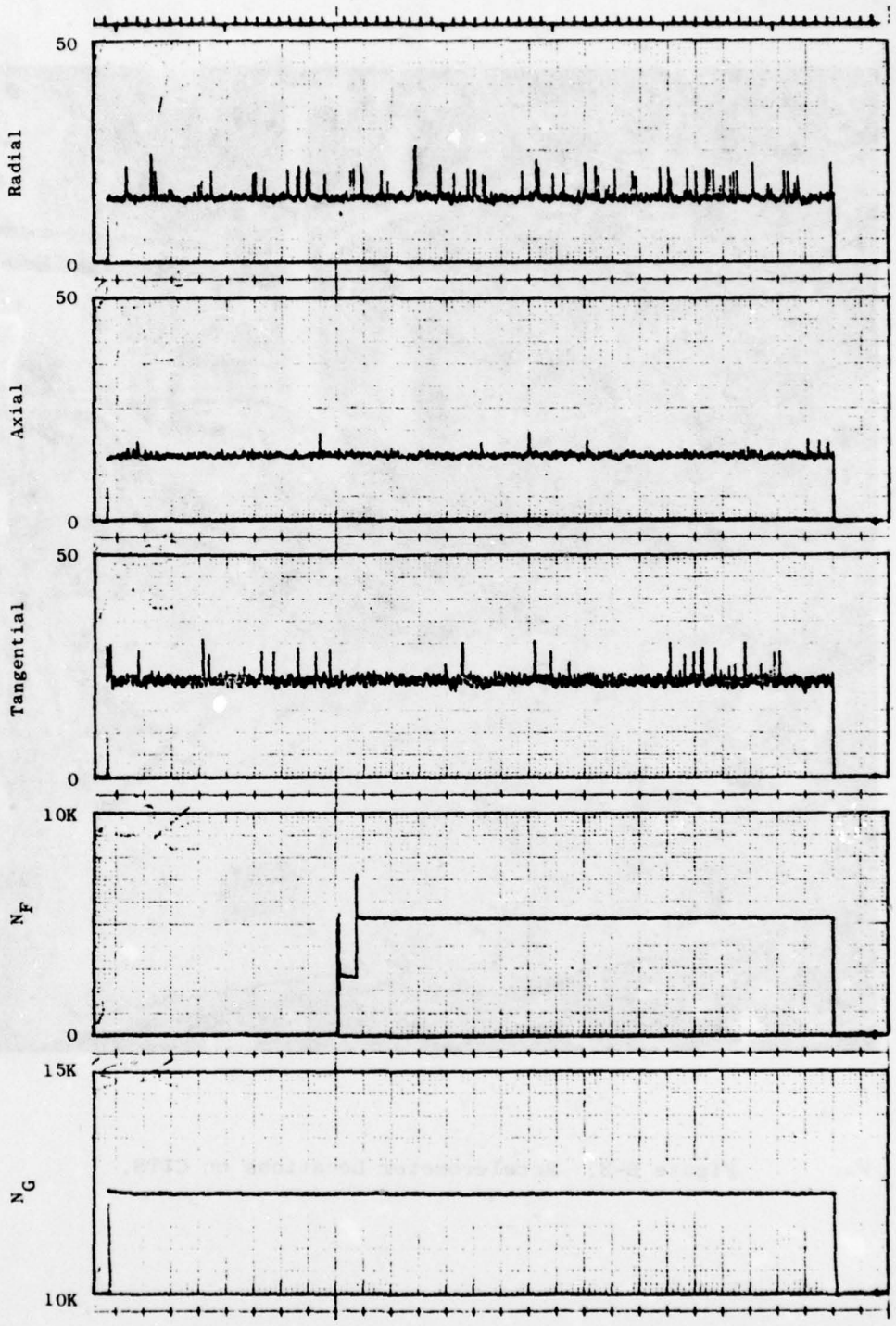


Figure B-4. F101 CITS Overall G-Level (69% Fan Speed).

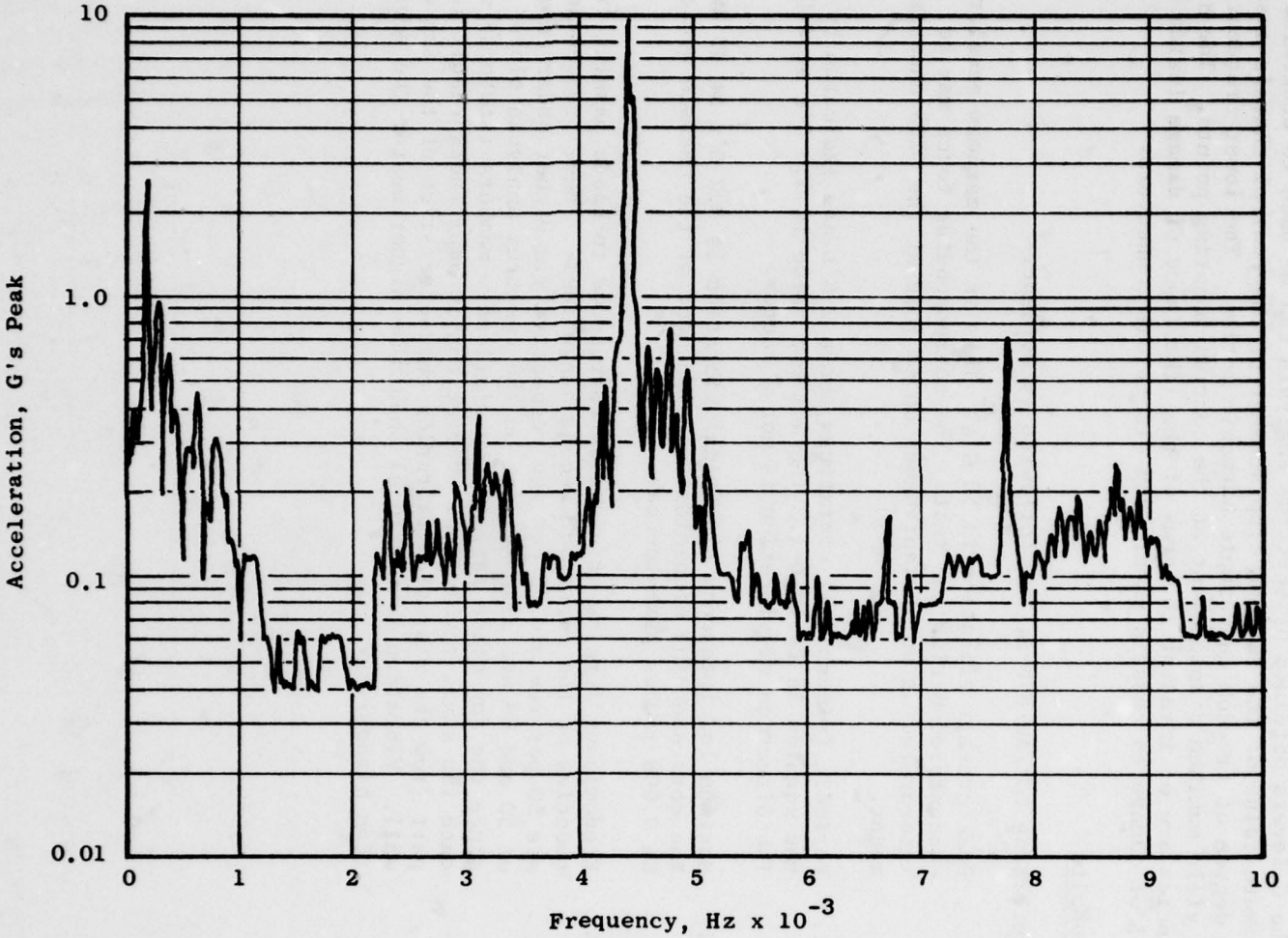


Figure B-5. Results of the Spectrum Analysis (69% Fan Speed).

bandwidth of 20 Hz. The average peak (maximum) G-level over each bandwidth is obtained from 256 scans of the frequency region.

The G-levels obtained by spectrum analysis can be used to determine an approximate value of the maximum displacement of the control chassis assuming single degree of freedom and simple harmonic motion. The lower frequencies should yield maximum displacement at the control mounting points. The higher frequencies are of interest in terms of the likelihood of damage inside the control or damage to chassis panels and electrical connectors.

5. Results

Referring to Table B-1, the following is evident:

1. Peak overall vibration is 50 G's. This is the maximum acceleration encountered during the test. The corresponding force may be interpreted as an instantaneous shock load at the CITS chassis mount.

2. Periodic (sinusoidal) vibrations above 2 G's are indicated by the squares in Table B-1. The maximum value is 9.8 G's at 4400 Hz. The direction of vibration is not a factor.

3. Maximum low frequency sinusoidal vibration is 3.2 G's at 88 Hz. The corresponding sinusoidal displacement of the chassis would be 0.008 inches peak-to-peak.

4. Predominant forcing frequencies correspond to blade passing frequencies of the first and second stage fans. These frequencies are 50 per rev and 88 per rev respectively. Higher order multiples of 50 and 88 are also evident on the spectrum analysis plots since the fan blade passes many stationary members (stators) during each fan shaft revolution. Variations in amplitudes result in part from the vibration filtering characteristics of the fan duct wall. Vibration levels (G's) should be higher nearer the source (fan blades).

Table B-1. F101 CITS Vibrations.

Core % (rpm)	Fan % (rpm)	Core 1/Rev (Hz)	Fan 1/Rev (Hz)	Fan 1st Stg. 50/Rev (Hz)	Fan 2nd Stg. 88/Rev (Hz)	Overall G's (peak)
72%	38%					
10350 rpm	2850 rpm	172 Hz	47 Hz	2375 Hz	4180 Hz	
Radial	G's	1.3	0.2	0.6	1.0	25
Axial	G's	0.8	0.3	0.5	0.6	15
Tangential	G's	0.3	0.4	0.4	1.6	22
74%	41%					
10760 rpm	3120 rpm	179 Hz	0.52 Hz	2600 Hz	4576 Hz	
Radial		1.2	0.4	0.12	0.7	20
Axial		1.2	0.3	1.0	0.3	15
Tangential		1.4	0.4	1.8	1.5	20
76%	51%					
11040 rpm	3880 rpm	184 Hz	65 Hz	3250 Hz	5720 Hz	
Radial		0.5	0.5	0.1	2.4	30
Axial		0.4	1.0	0.1	1.8	25
Tangential		0.2	0.6	0.6	2.1	35
86%	69%					
12500 rpm	5250 rpm	208 Hz	88 Hz	4400 Hz	7744 Hz	
Radial		2.1	2.8	4.0	0.4	22
Axial		0.8	3.2	6.0	0.2	17
Tangential		2.4	0.4	9.8	0.7	30
83%	71%					
12030 rpm	5350 rpm	200 Hz	89 Hz	4458 Hz	7832 Hz	
Radial		1.2	1.7	2.3	1.1	30
Axial		1.0	2.6	0.8	0.3	23
Tangential		0.7	2.1	3.8	1.9	30
93%	89%					
13500 rpm	6750 rpm	225 Hz	112 Hz	5625 Hz	9900 Hz	
Radial		0.5	2.7	3.0	2.3	25
Axial		0.8	2.9	4.7	1.3	23
Tangential		0.8	1.9	2.2	1.5	26
93%	90%					
13400 rpm	6800 rpm	223 Hz	113 Hz	5667 Hz	9773 Hz	
Radial		0.9	0.5	6.2	0.9	40
Axial		2.6	2.6	4.9	0.5	50
Tangential		0.8	0.9	3.6	0.3	35
97%	94%					
1400 rpm	7140 rpm	223 rpm	119 Hz	5950 Hz	10742 Hz	
Radial		0.6	2.7	4.5	---	30
Axial		0.7	2.6	1.8	---	25
Tangential		0.7	1.8	2.6	---	25
99%	99%					
14330 rpm	7520 rpm	239 Hz	125 Hz	6267 Hz	11029 Hz	
Radial		0.5	0.8	5.1	---	35
Axial		1.2	2.0	2.1	---	50
Tangential		0.6	0.7	6.0	---	35

Note: Core 100% = 14460 rpm
Fan 100% = 7570 rpm
Fan 1st Stage = 50 Blades
Fan 2nd Stage = 88 Blades

APPENDIX C - HEAT TRANSFER ANALYSES

1. Temperature Gradients

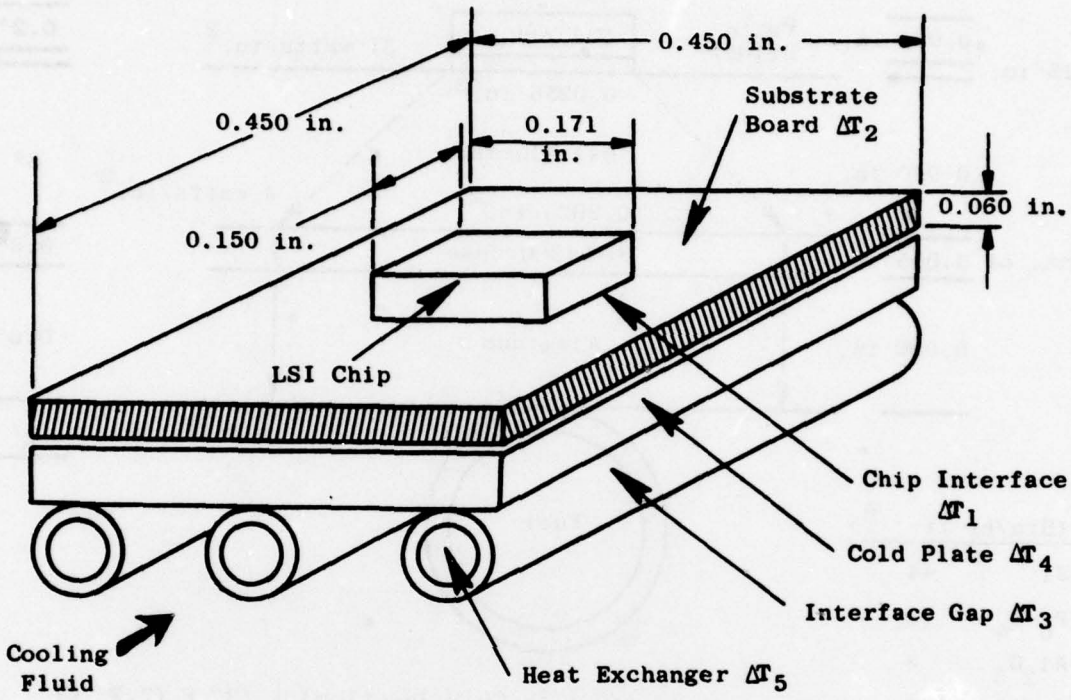
Calculations were made of the temperature gradients form the fuel to the chip. Figure C-1 shows the significant temperature gradients involved and the dimensions of the heat transfer paths. Figure C-2 shows the maximum values of temperature rise for a 0.8-watt LSI memory chip. These results were obtained by hand-calculations using conventional formulas for heat transfer by forced convection, one-dimensional conduction, and two-dimensional heat spreading.

Fuel is assumed to flow through a plain, 0.250-inch-diameter x 0.020-inch-wall thickness, aluminum tube brazed to the underside of a 0.090-inch-thick aluminum plate. The rows of the serpentine-shaped cooling tubes are spaced one inch apart.

The 0.090-inch-thick aluminum on the cold plates acts as an effective heat spreader with only 0.6° F temperature rise at heat flux of 4 $W/in.^2$ for the LSI chip. The heat-transfer grease, G-642, has a thermal conductivity value 40 times better than air and about six times better than most non-metallic compounds such as RTV. A thickness of 0.005 inch is used for analysis but this can be reduced to 0.0025 inch based on the flatness requirements of the substrate board and cold plate.

Any means for mounting high-power, hybrid substrates other than directly over a liquid-cooled heat exchanger would be at considerable sacrifice to temperature rise by conduction. If the cooling path were lengthwise rather than across the cold plate, the temperature rise would increase by the square of the distance from the chip to the heat sink. For example, at 4 $W/in.^2$, a 0.25-inch-thick x 3-inch-long plate produces a ΔT of 37.8° C.

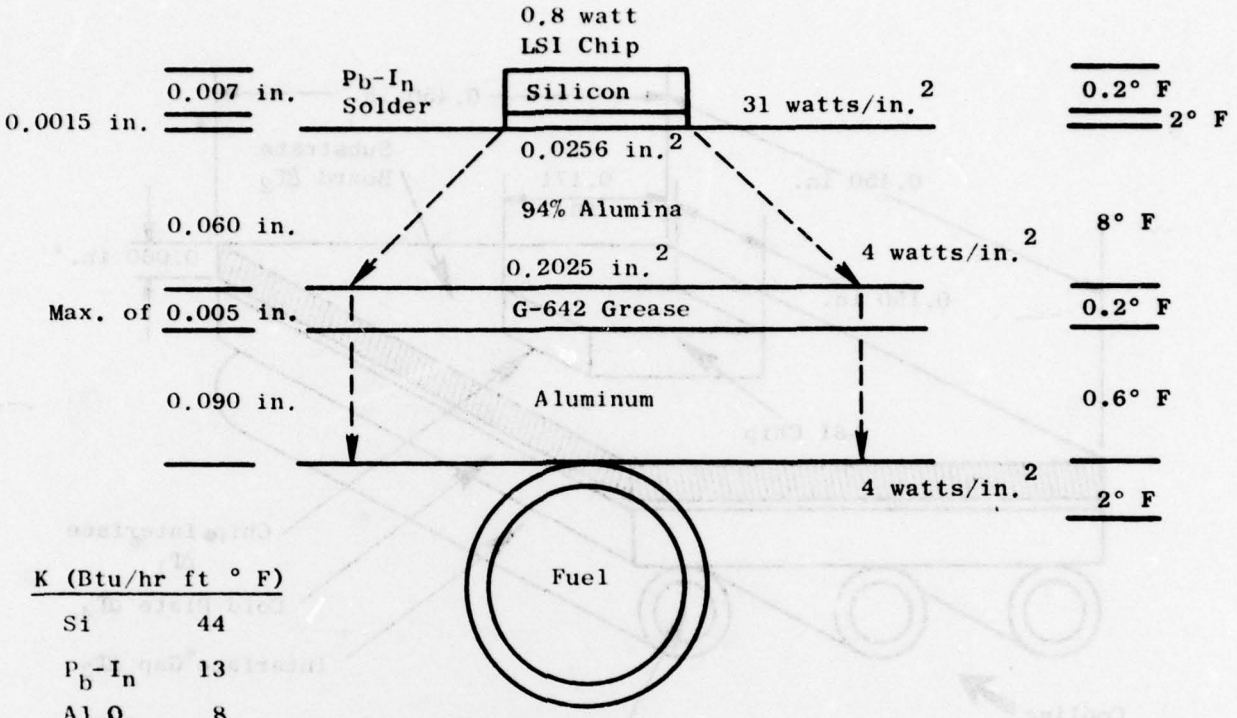
It is very important that the substrate board material have high thermal conductivity in order to rapidly spread heat and reduce the heat flux as it flows from the chip toward the heat sink. For the 0.8-watt LSI chip, heat flux is 31 $W/in.^2$ directly below the chip but dissipates to 4 $W/in.^2$ by the time the heat reaches the grease film. Figure C-3 shows a comparison of heat spreading versus no heat spreading in the substrate. The grease layer would be applied by roller to the bottom of the hybrid board to obtain a thin, uniform coating. Grease retention would be due to high viscosity (no damming required). This same material has been used for mounting high-power, stud-mounted components and module cans to chassis. Satisfactory retention and stability have been demonstrated under higher squeeze, and over the temperature range, expected.



ΔT Chip Junction → Cooling Fluid Inlet =

ΔT_1 Chip-to-Substrate Interface
ΔT_2 Heat Spreading in Substrate Board
ΔT_3 Substrate-to-Cold-Plate Interface
ΔT_4 Aluminum Cold Plate
ΔT_5 Heat Exchanger

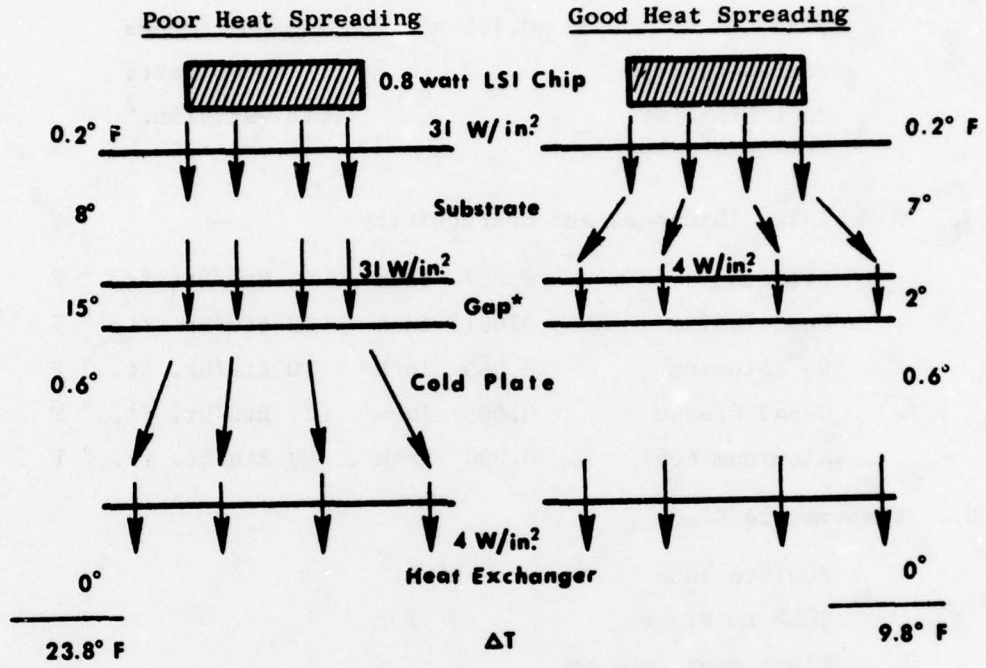
Figure C-1. Significant Temperature Gradients Considered in Cooling Hybrid Chip.



K (Btu/hr ft ° F)	
Si	44
P_b-I_n	13
Al_2O_3	8
G-642	0.7
Al	99

ΔT (Fuel to Chip Junction) = 13° F (7.2° C)

Figure C-2. Typical Maximum Thermal Gradients in Hybrid Board Using Aluminum Oxide Substrate at Four Watts Per Square Inch.



* 0.008-in. Gap of G-642 Grease

Figure C-3. Effect of Heat Spreading on ΔT Across Substrate/Cold Plate Gap.

2. Computer Thermal Analysis

A LSI chip and alumina substrate were modeled using the Transient Heat Transfer Temperature Distribution (THTD) computer program. This is a finite element analyses which iterates the heat flux into and out of modes representing the geometry of the problem. The results are shown by Figure C-4 and the data given below:

a. Chip

Size	0.175 x 0.206 x 0.007 inches
Heat Generated	0.75 watts
Heat Flux (at bottom of chip)	20.8 watts/in.^{2}

b. Materials, Thickness and Conductivity

Silicon	0.007 inch	44 Btu/hr. ft. ° F
Lead-Indium	0.0015 inch	13 Btu/hr. ft. ° F
94°/Alumina	0.060 inch	10 Btu/hr. ft. ° F
G-642 Grease	0.005 inch	0.7 Btu/hr. ft. ° F
Aluminum 6061	0.090 inch	99 Btu/hr. ft. ° F

C. Temperature Rise

Fuel to Tube	0° F
Tube to Plate	1° F
Plate over Tube to Plate under Chip	8° F
Across Grease	5° F
Bottom of Substrate to Top of Substrate	3° F
Across Chip and Solder	0
Total	17° F

The largest rise is through the plate. It was estimated that the total temperature rise would be reduced from 17° F to 11° F if the tube were located directly under the chip.

The results indicate that the heat flux through the grease film is approximately five times greater directly under the chip than under the substrate area surrounding the chip. The temperature spreading behavior of

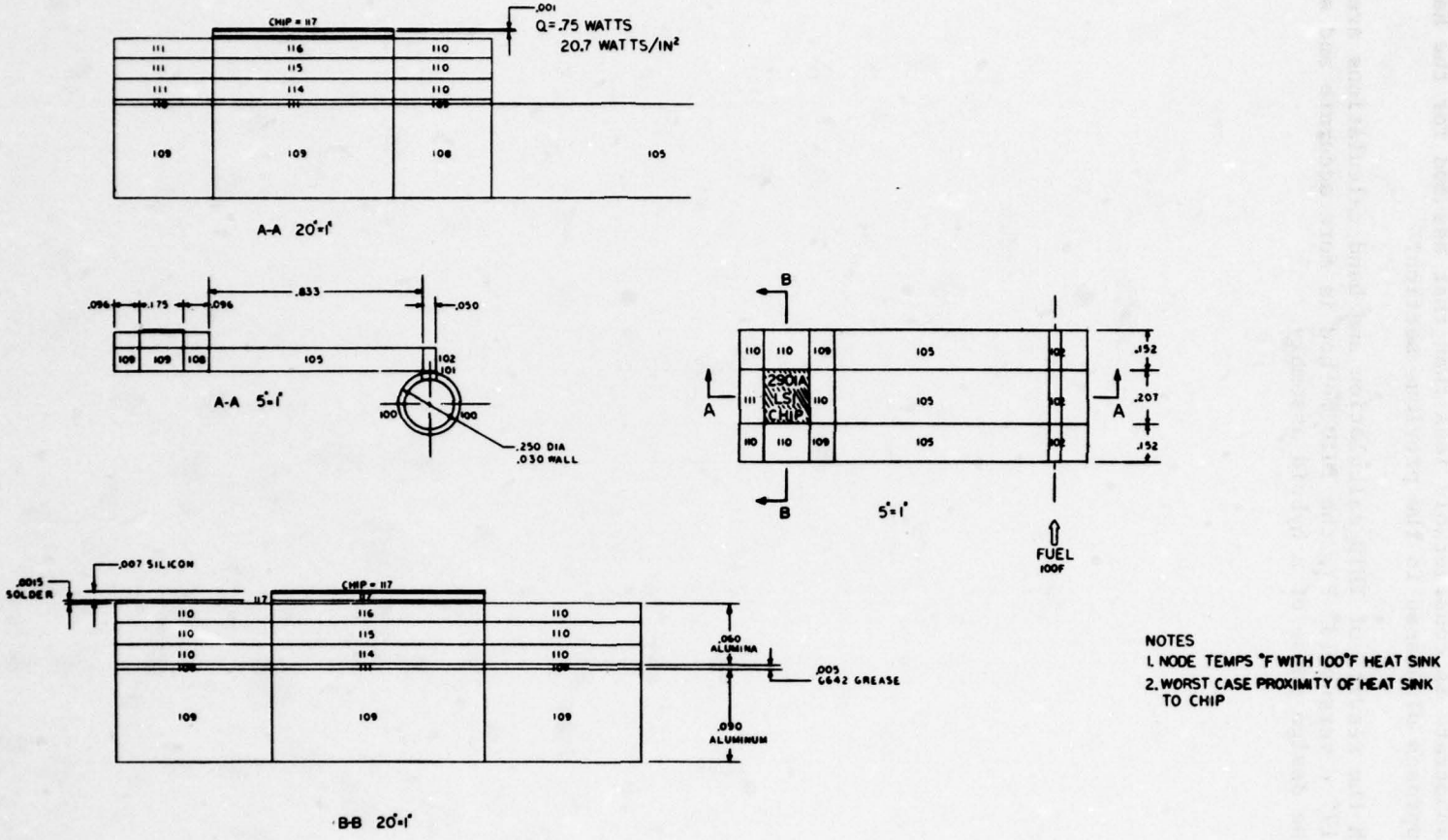
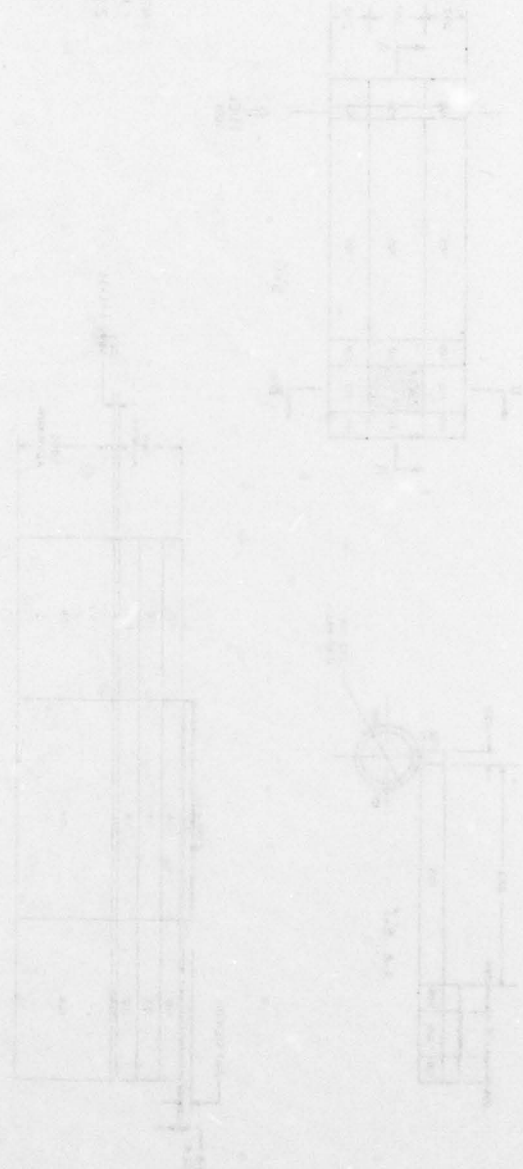


Figure C-4. Thermal Model.

the alumina substrate is considerably less than that assumed for the hand calculated approach disucssed in the previous section.

Although the results of THTD calculation and hand calculations are comparable (17° F versus 13° F), the THTD method is more accurate and should be used in the design phase of a hybrid assembly.



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